

FIG. 1

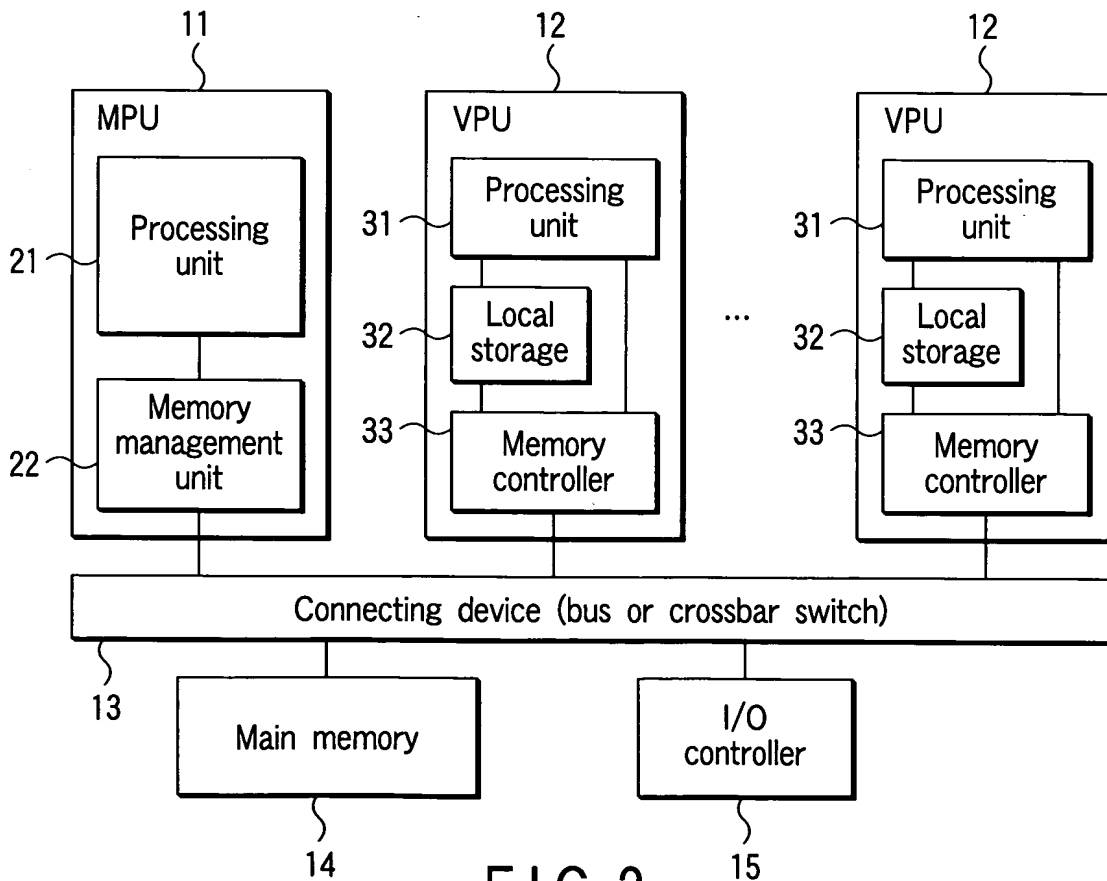


FIG. 2

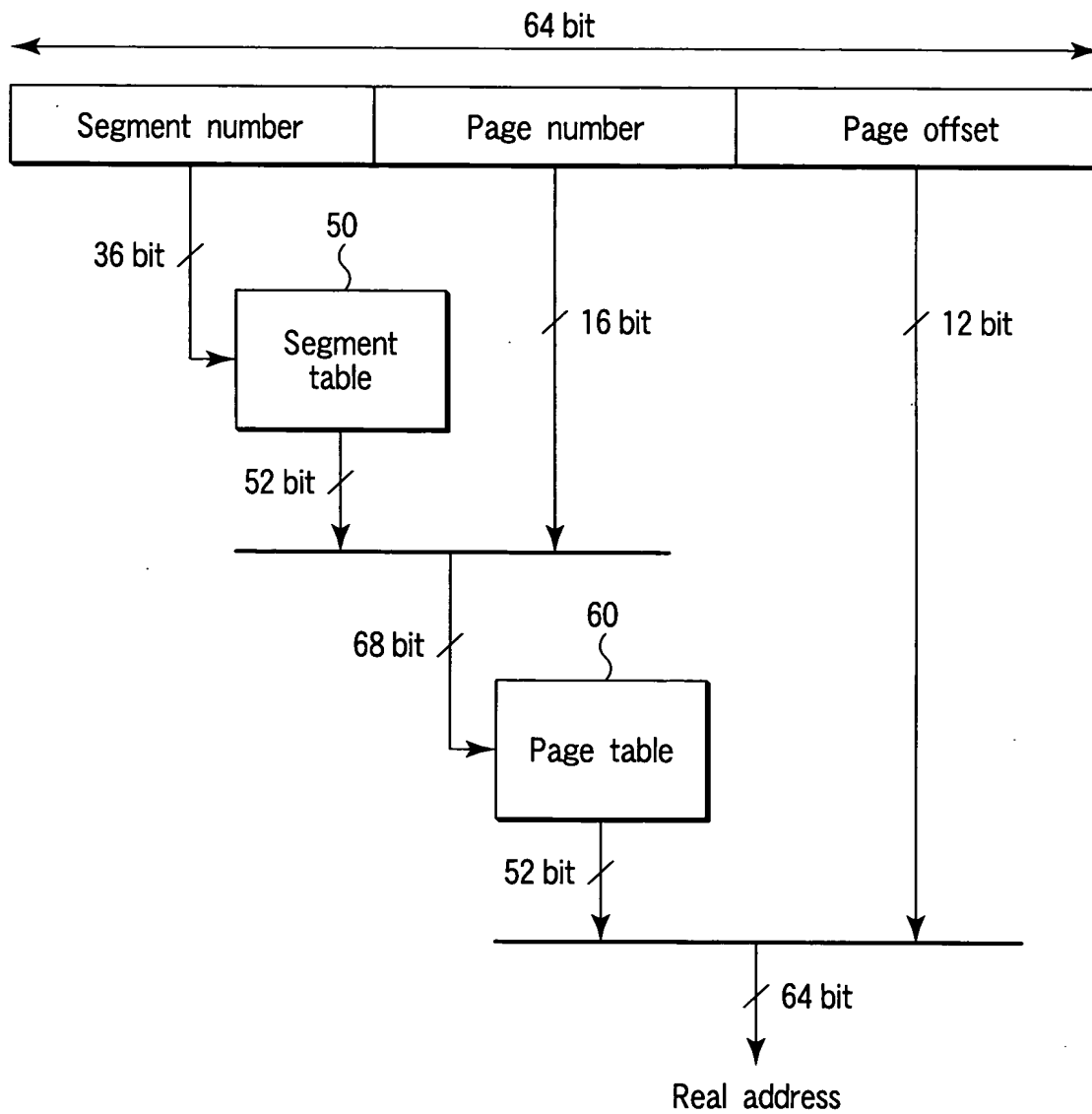


FIG. 3

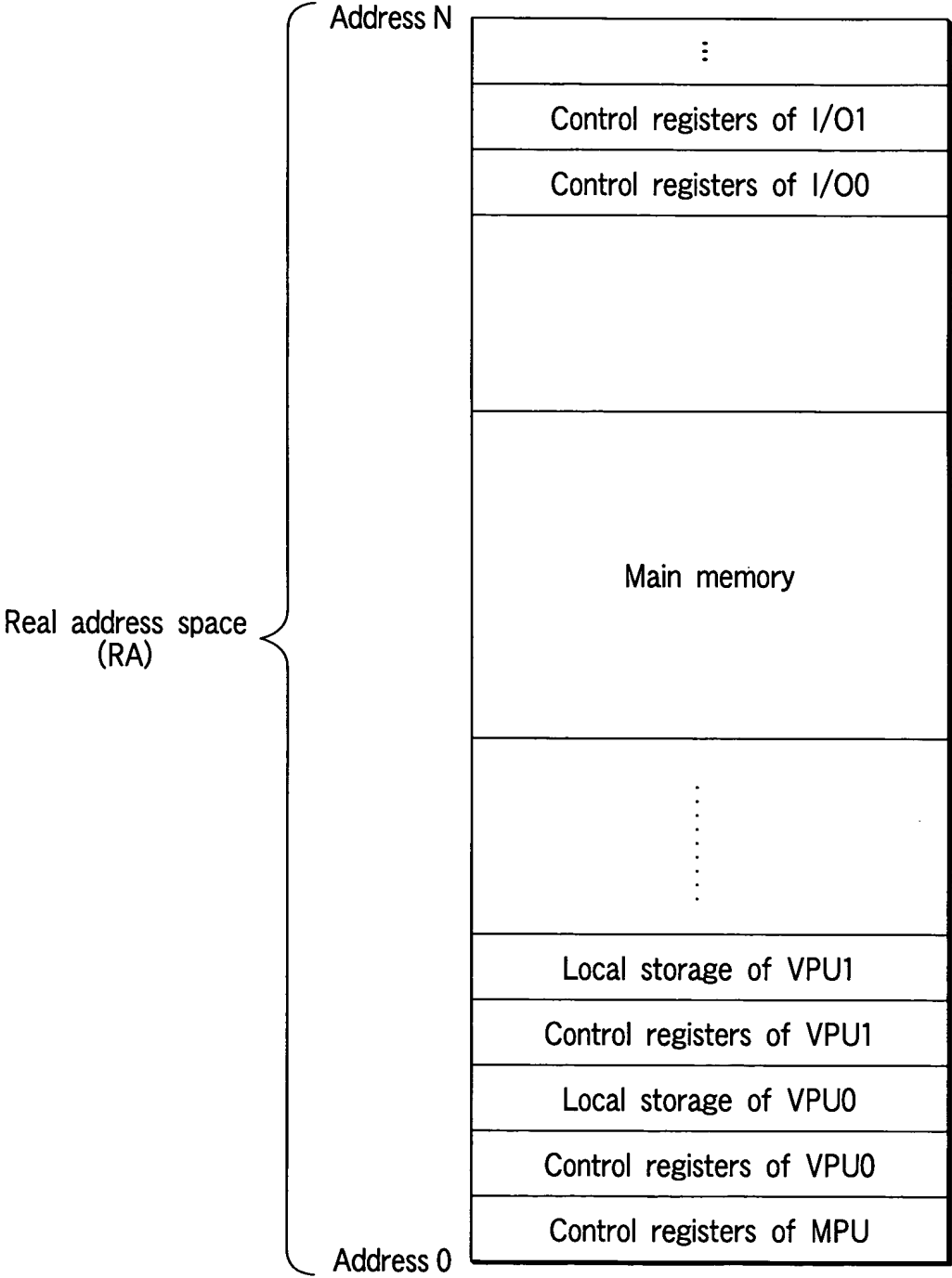


FIG. 4

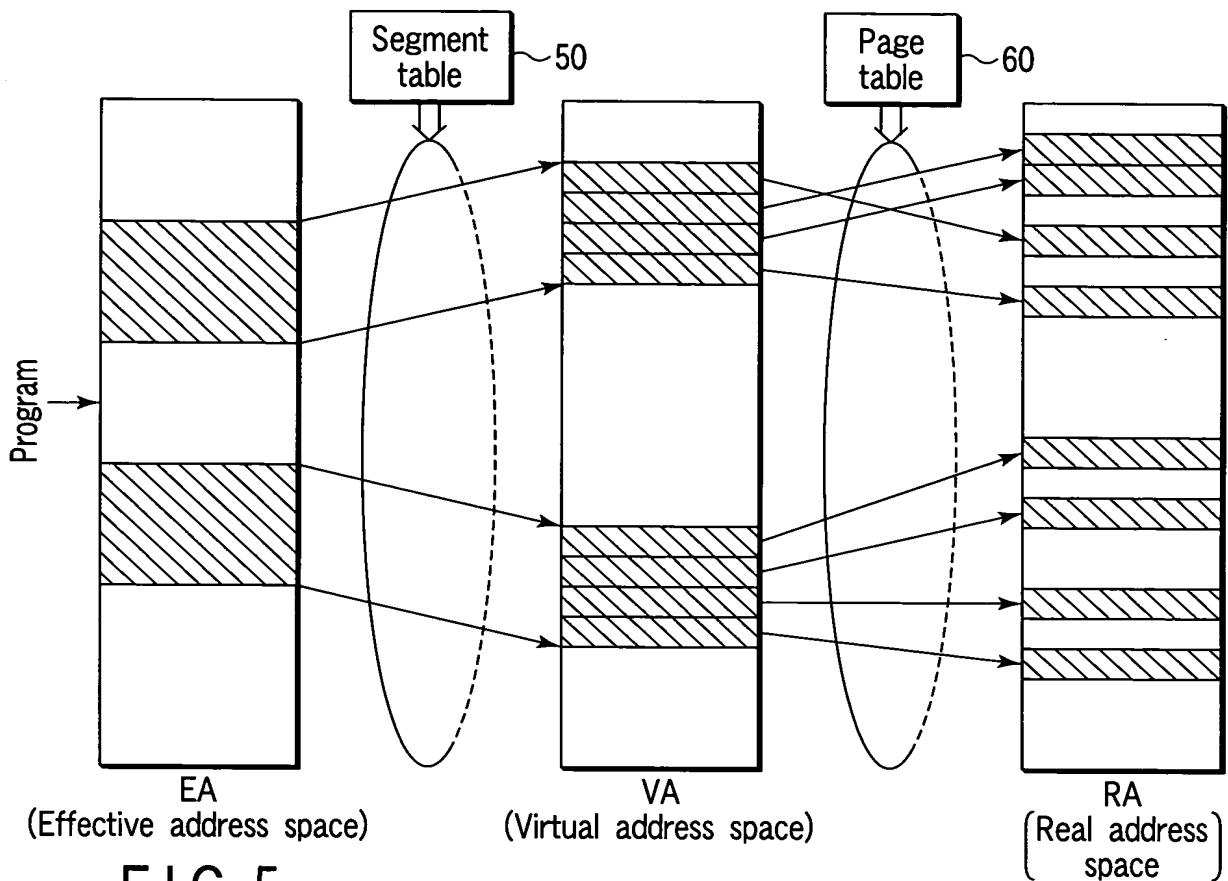


FIG. 5

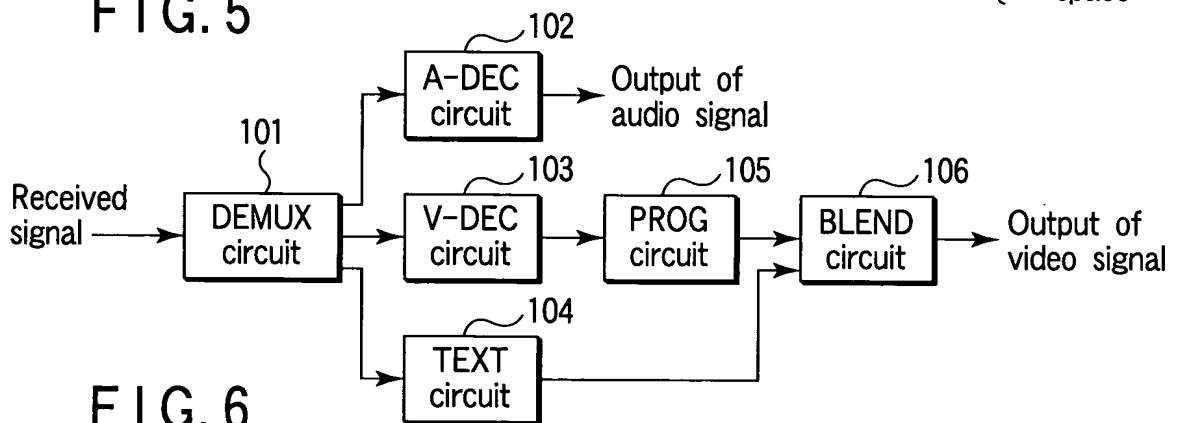


FIG. 6

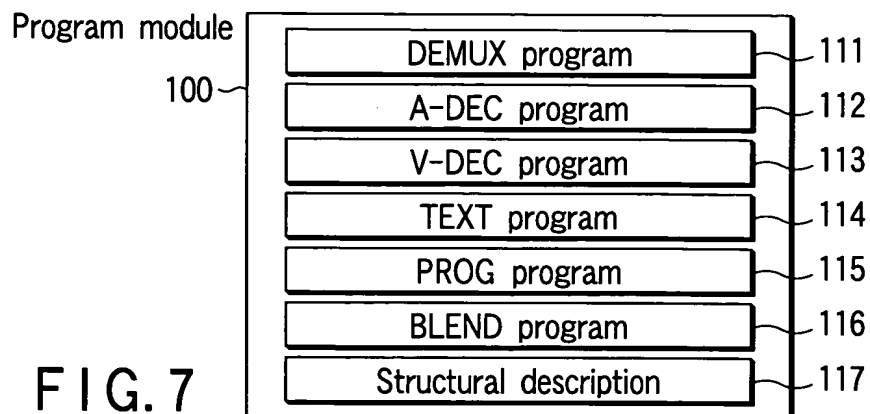


FIG. 7

Structural description 117

Number	Program	Input	Output	Cost	Buffer
(1)	DEMUX	Received signal	(2) (3) (4)	5	100KB 1MB 10KB
(2)	A-DEC	(1)	Audio output	10	_____
(3)	V-DEC	(1)	(5)	50	1MB
(4)	TEXT	(1)	(6)	5	10KB
(5)	PROG	(3)	(6)	20	1MB
(6)	BLEND	(4) (5)	Video output	10	_____
<p>Thread parameters</p> <p>(• Tightly coupled thread group :) (• Loosely coupled thread group :)</p>					
<p>Others</p>					

FIG. 8

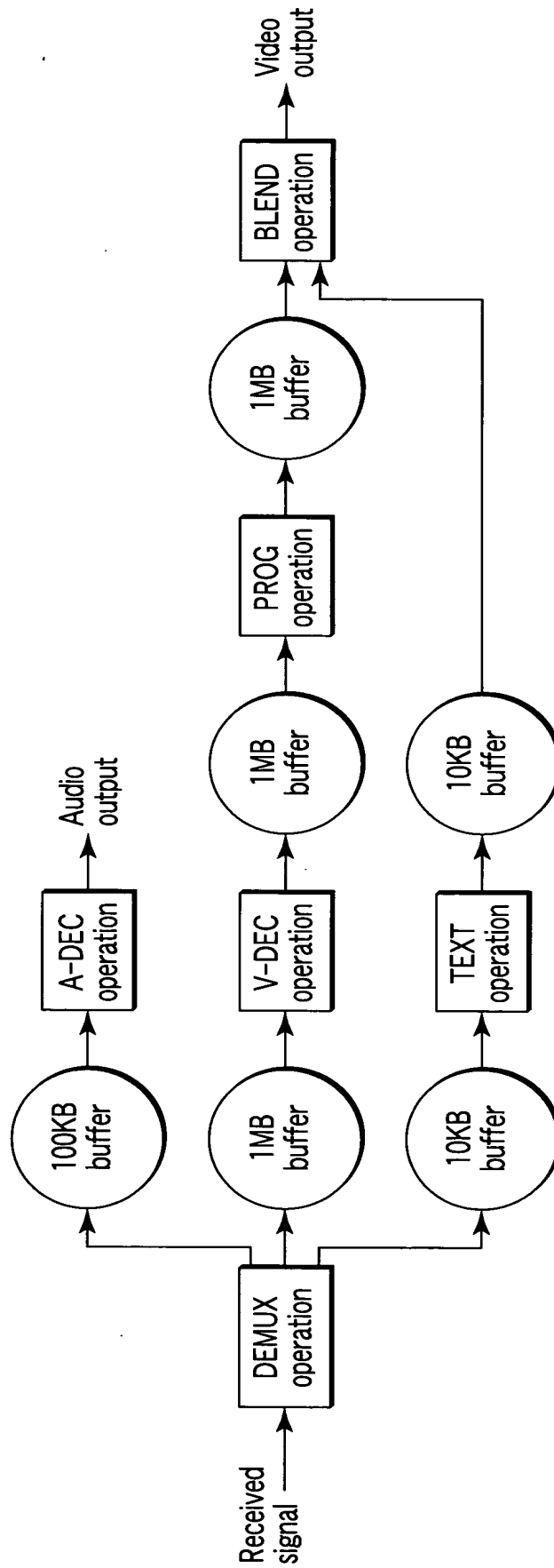


FIG. 9

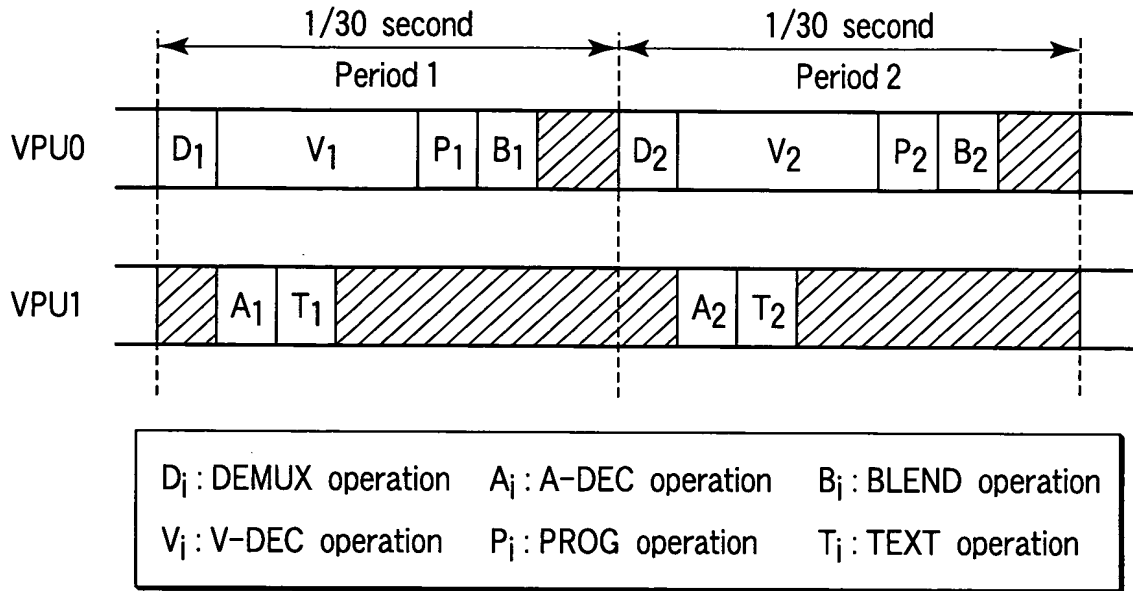


FIG. 10

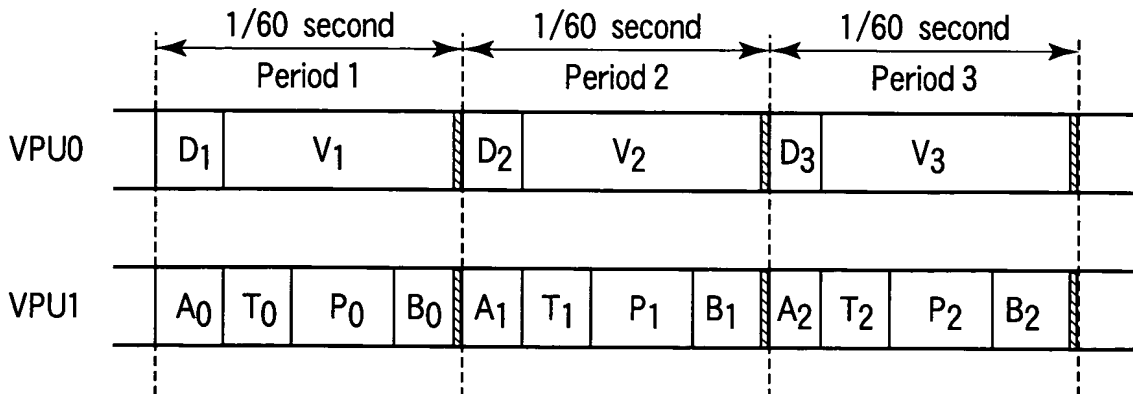


FIG. 11

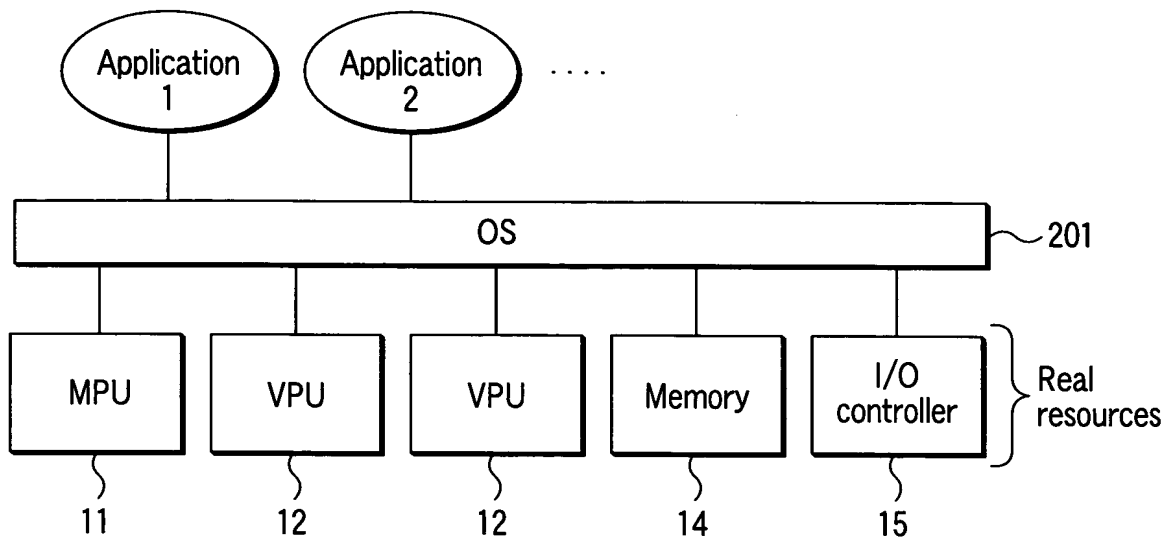


FIG. 12

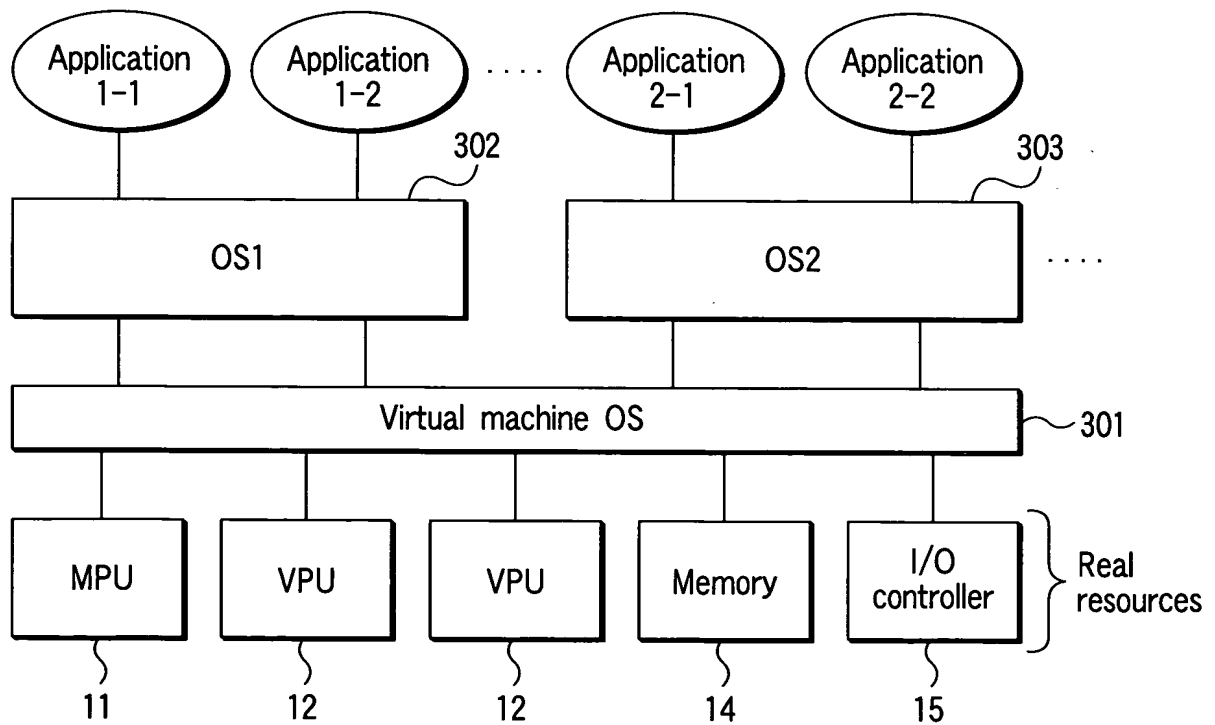


FIG. 13

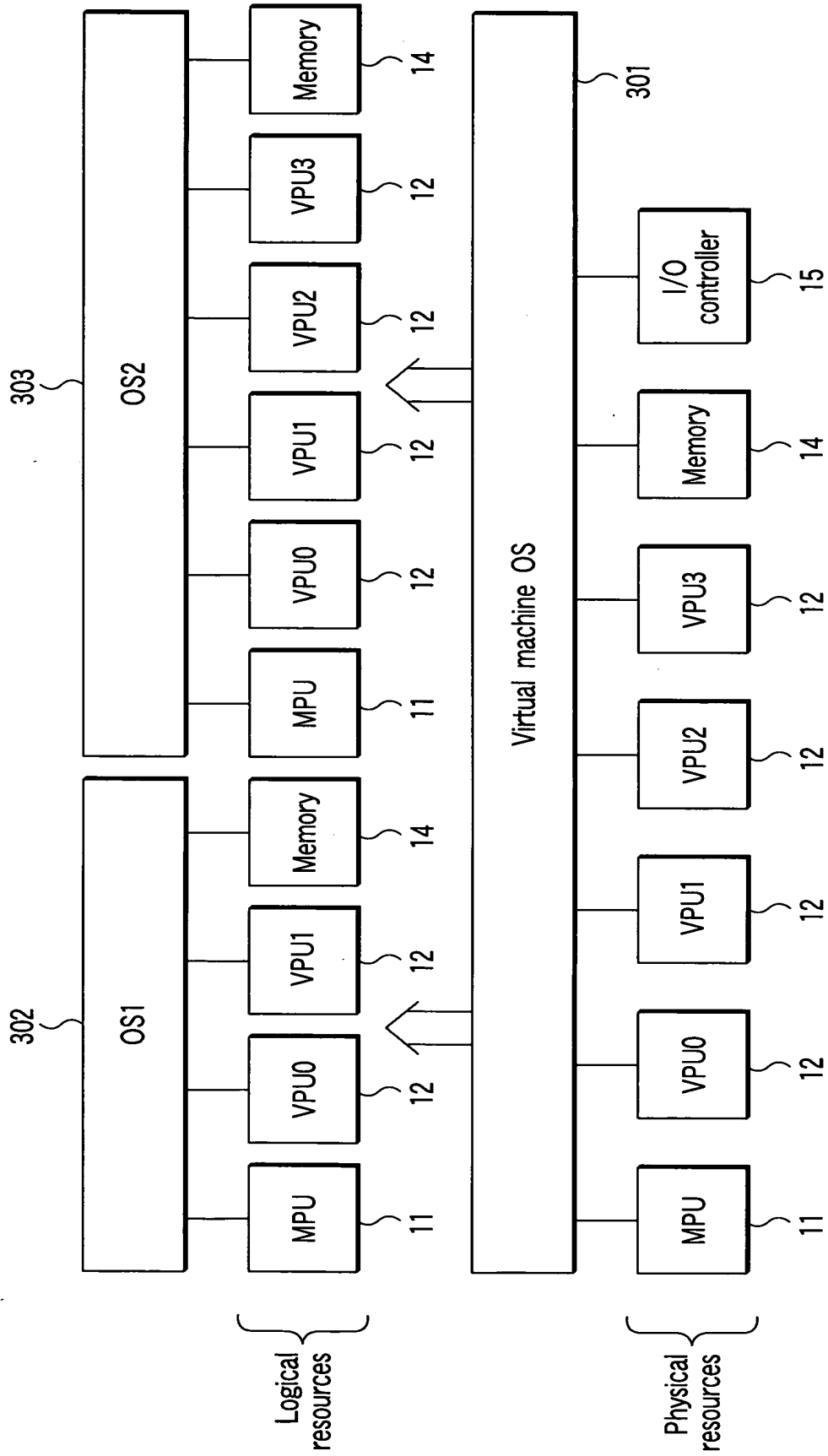


FIG.14

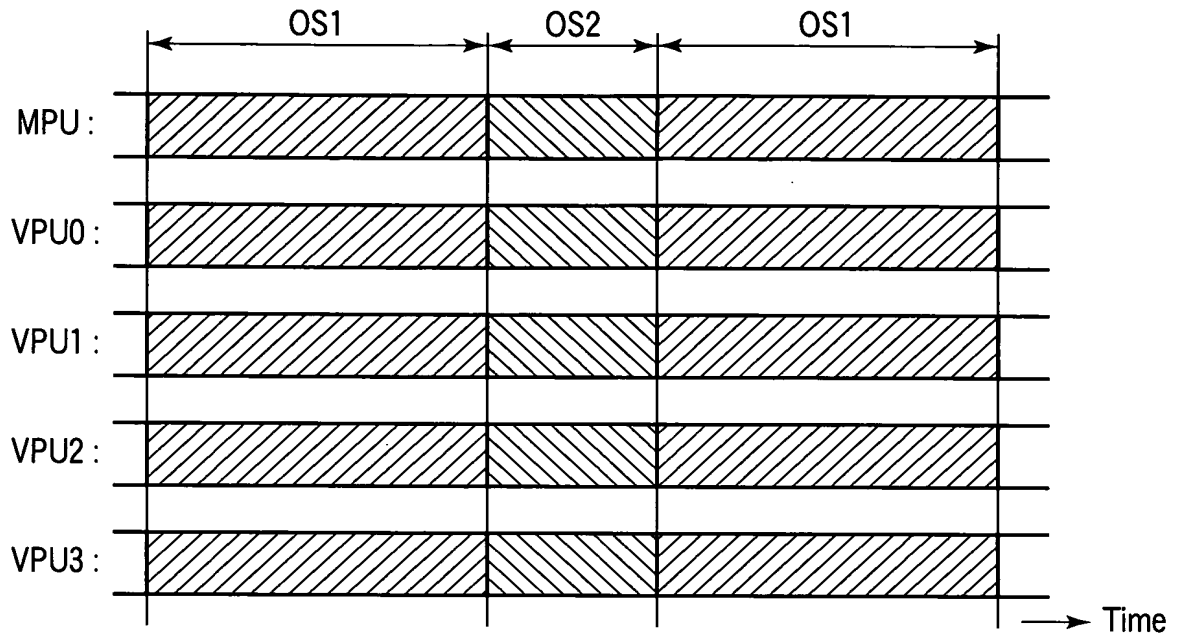


FIG. 15

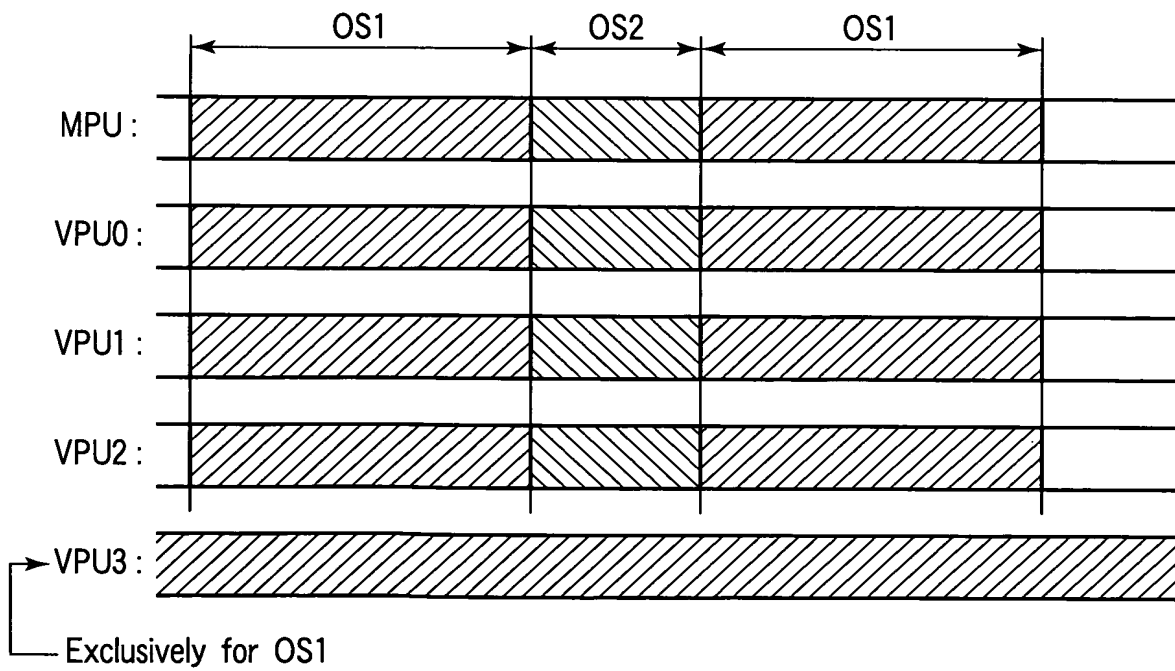


FIG. 16

FIG. 17

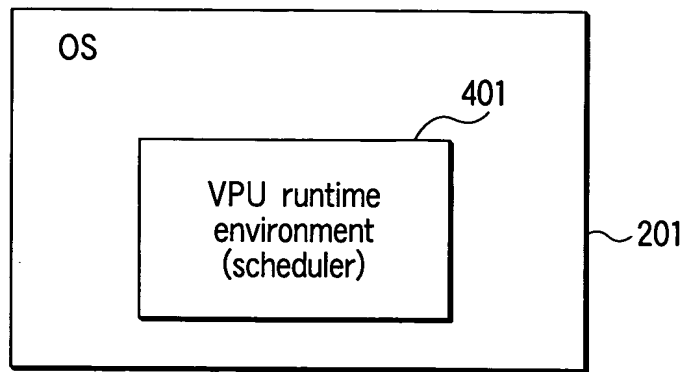


FIG. 18

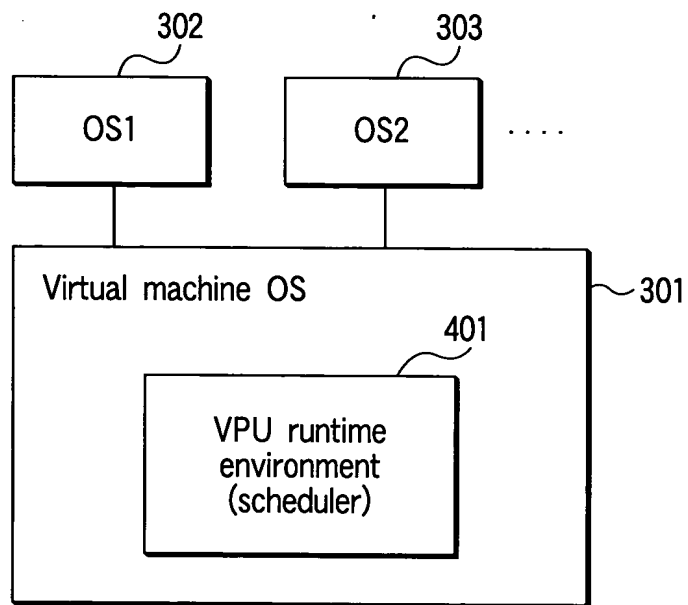
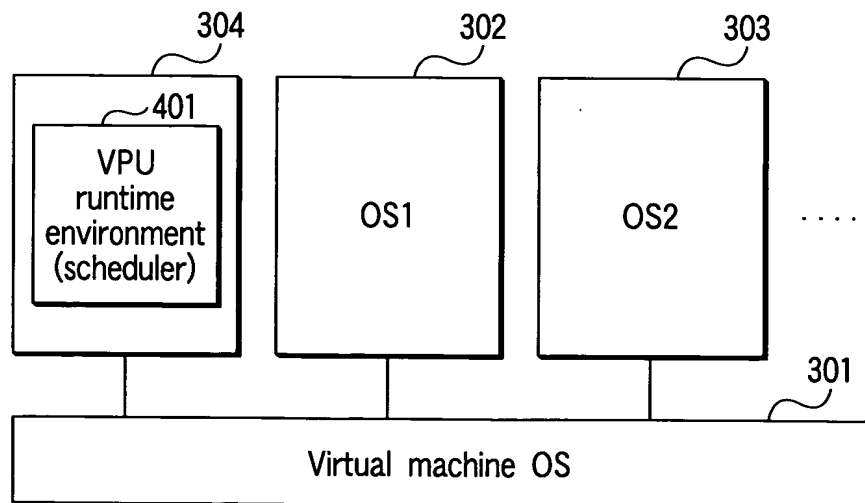


FIG. 19



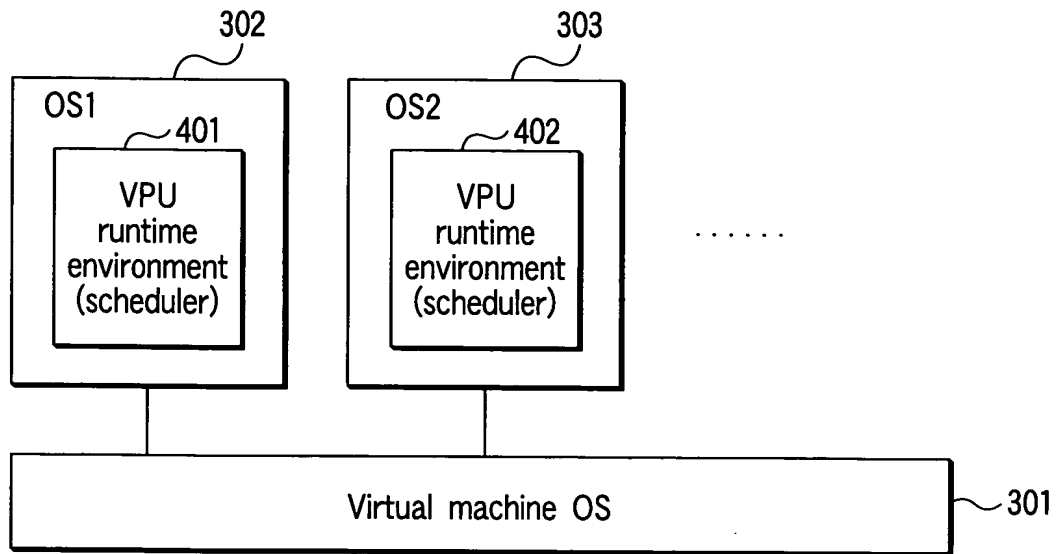


FIG. 20

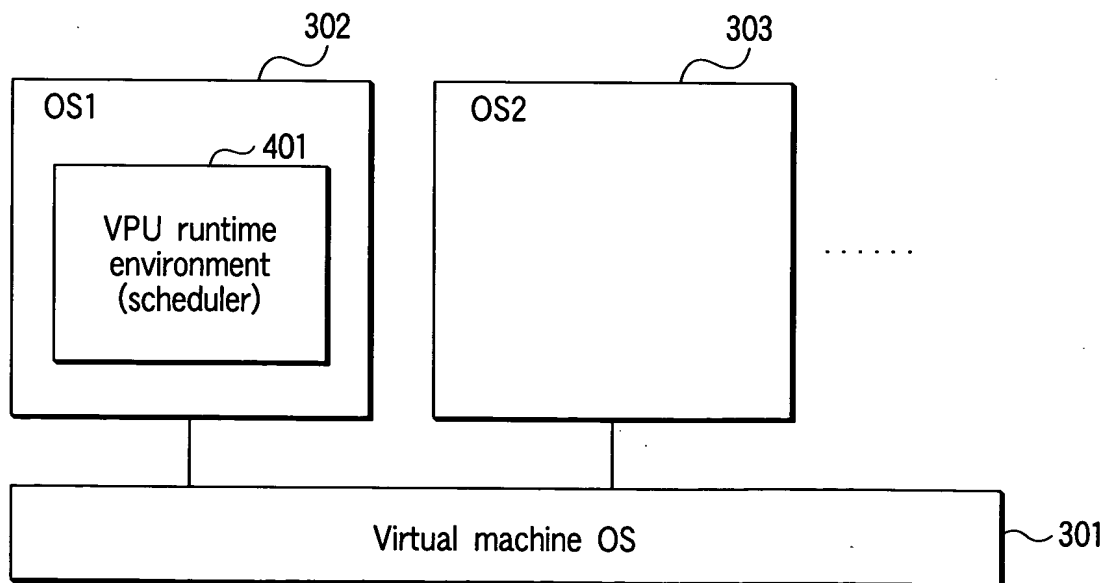


FIG. 21

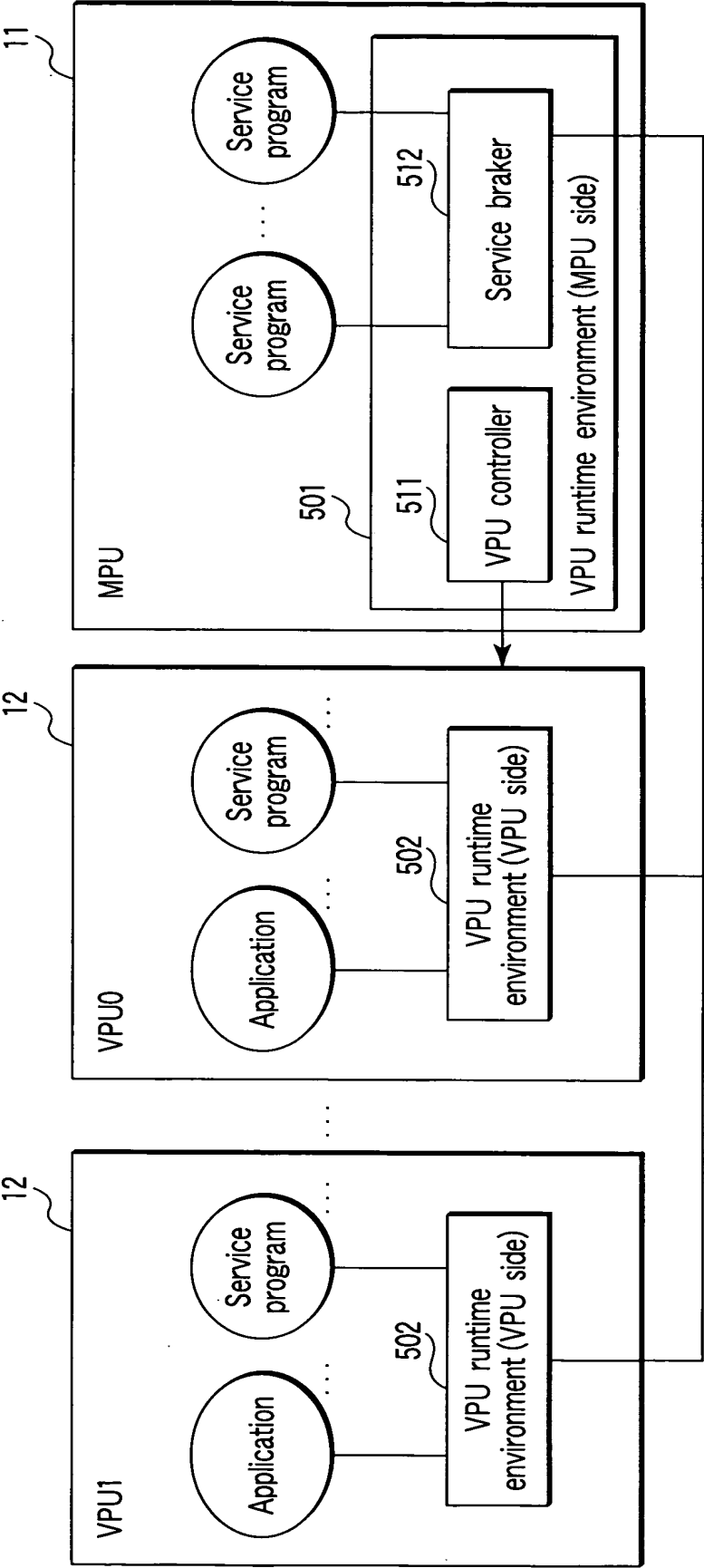
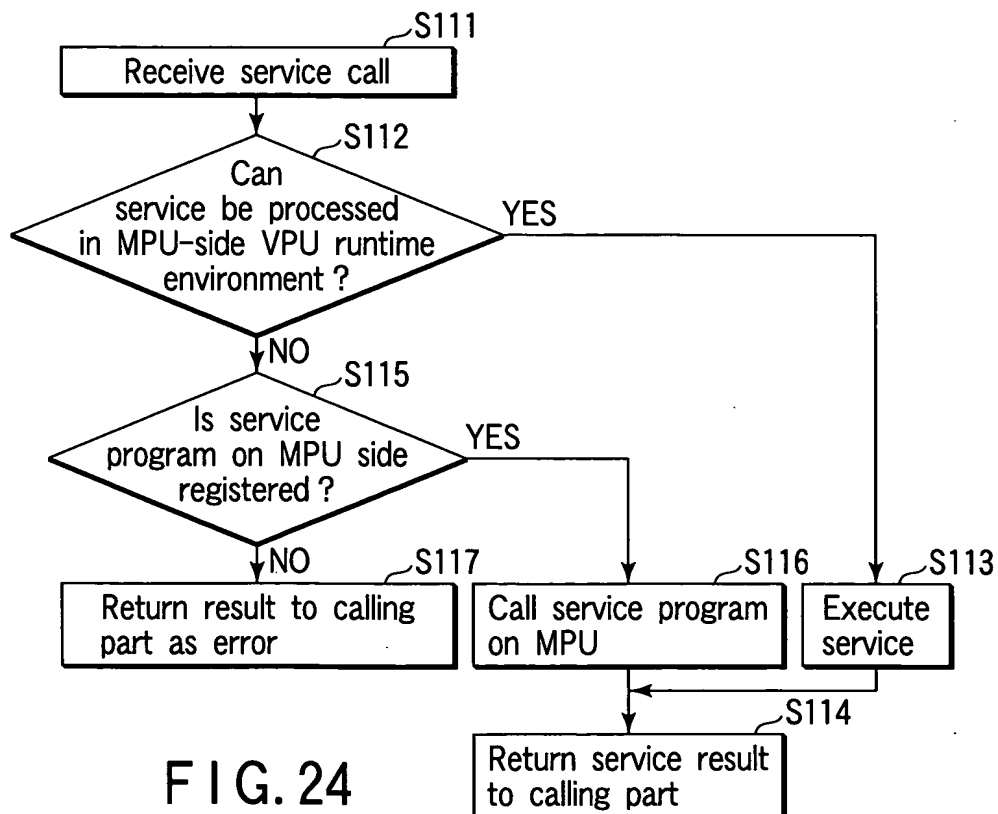
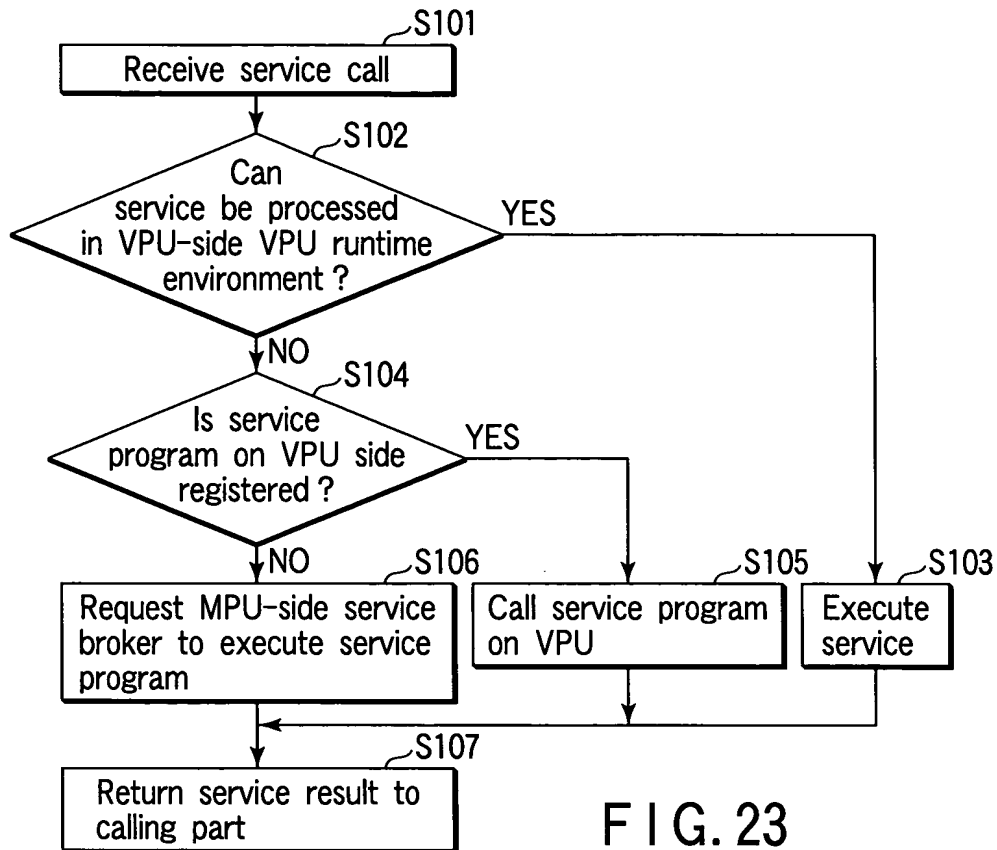


FIG. 22



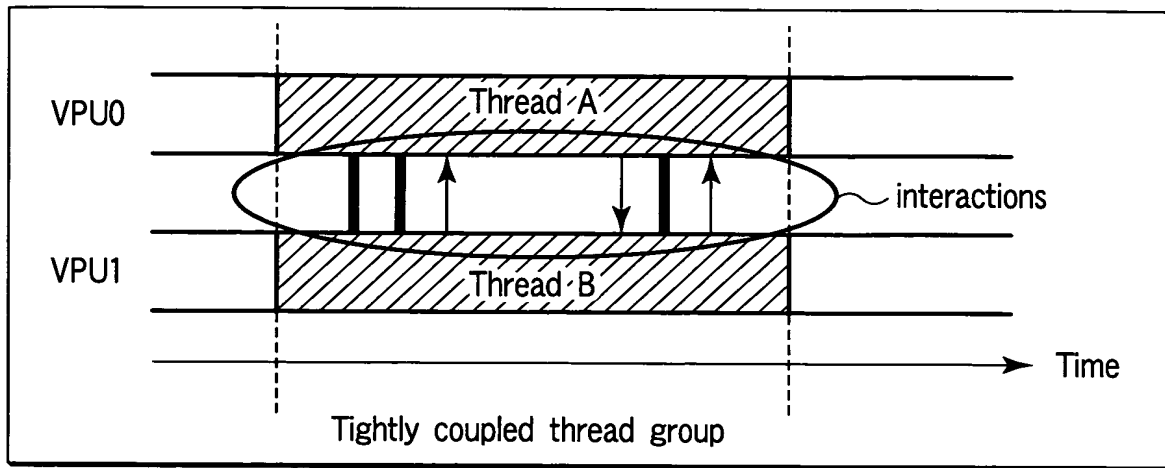


FIG. 25

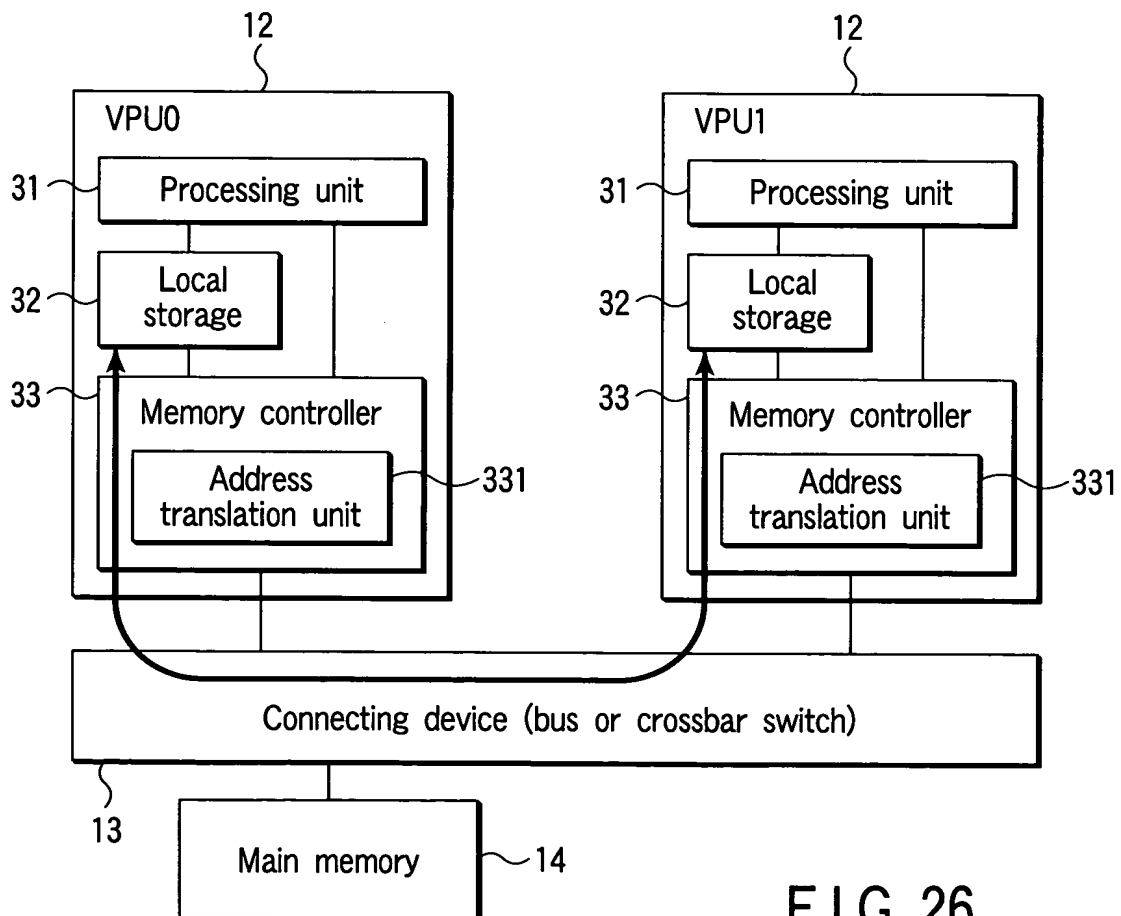


FIG. 26

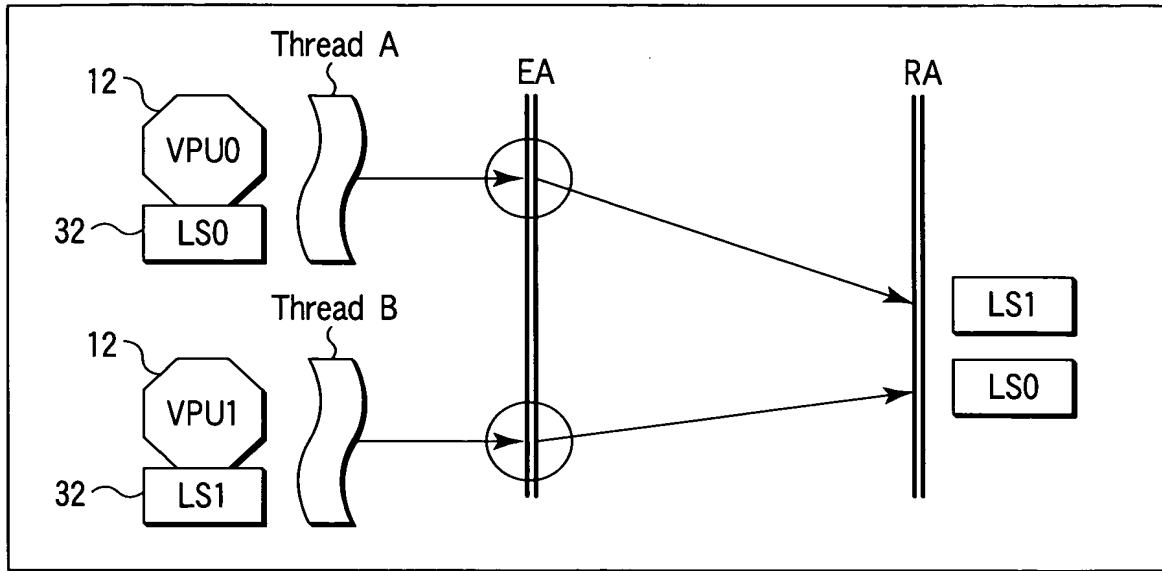


FIG. 27

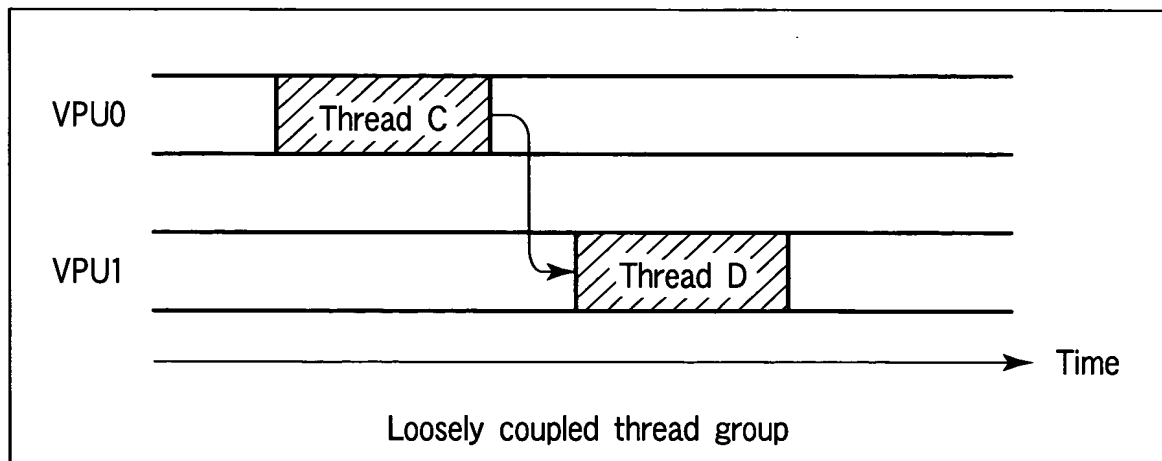


FIG. 28

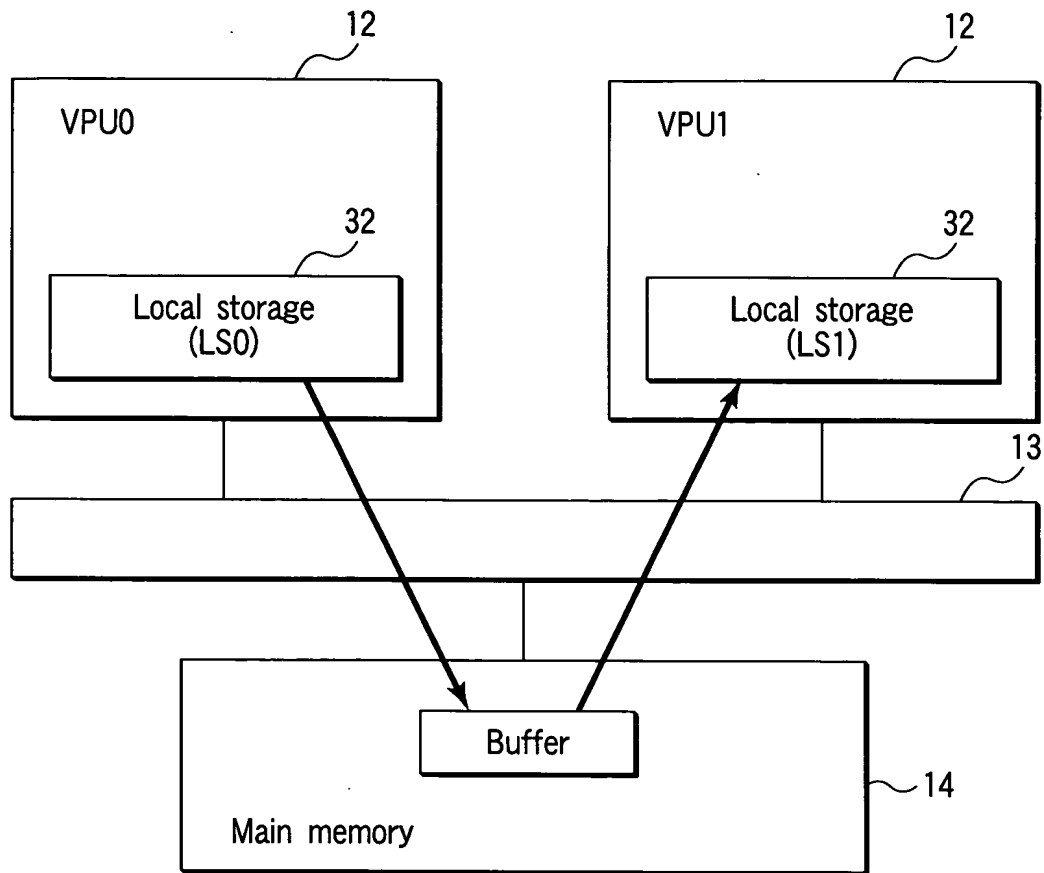


FIG. 29

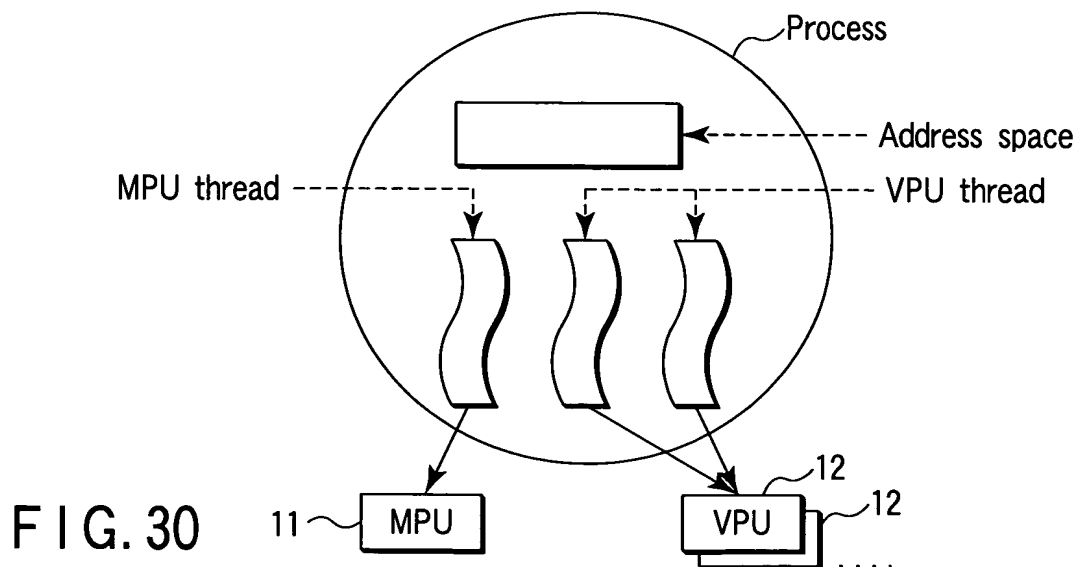


FIG. 30

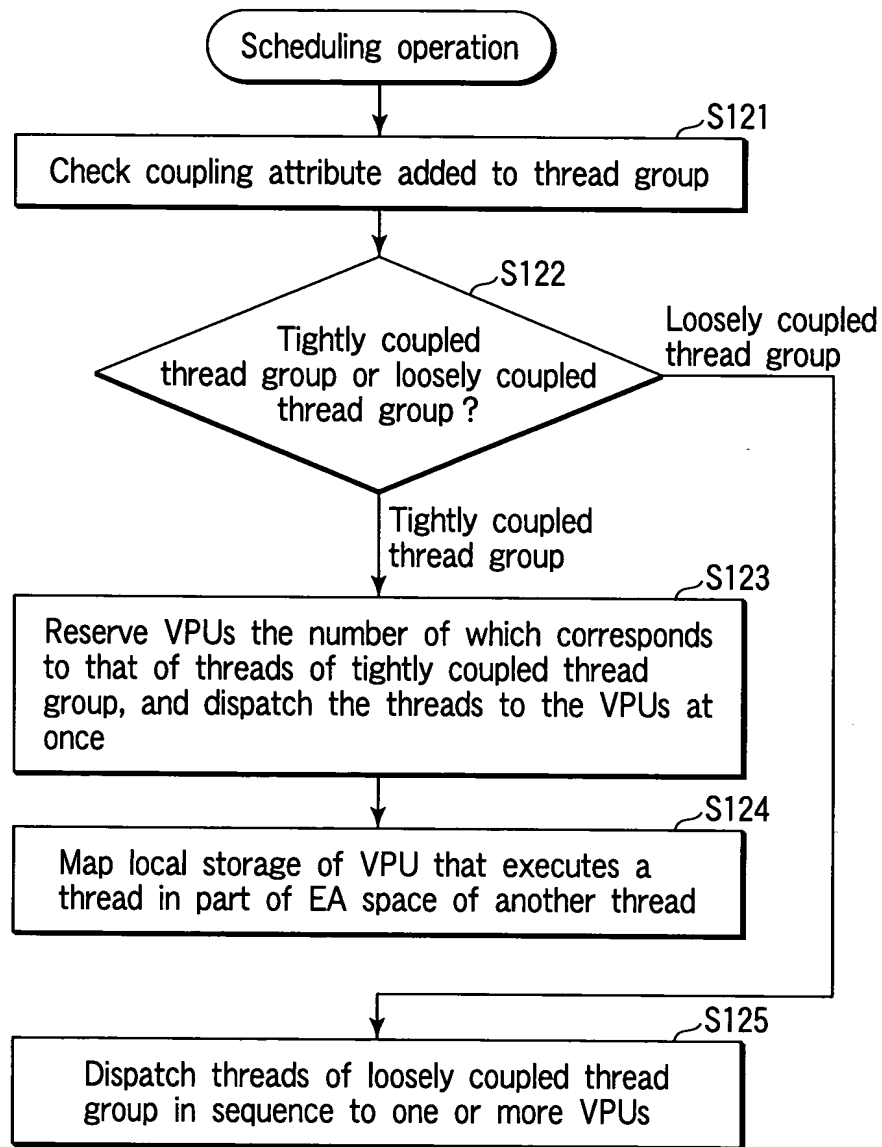


FIG. 31

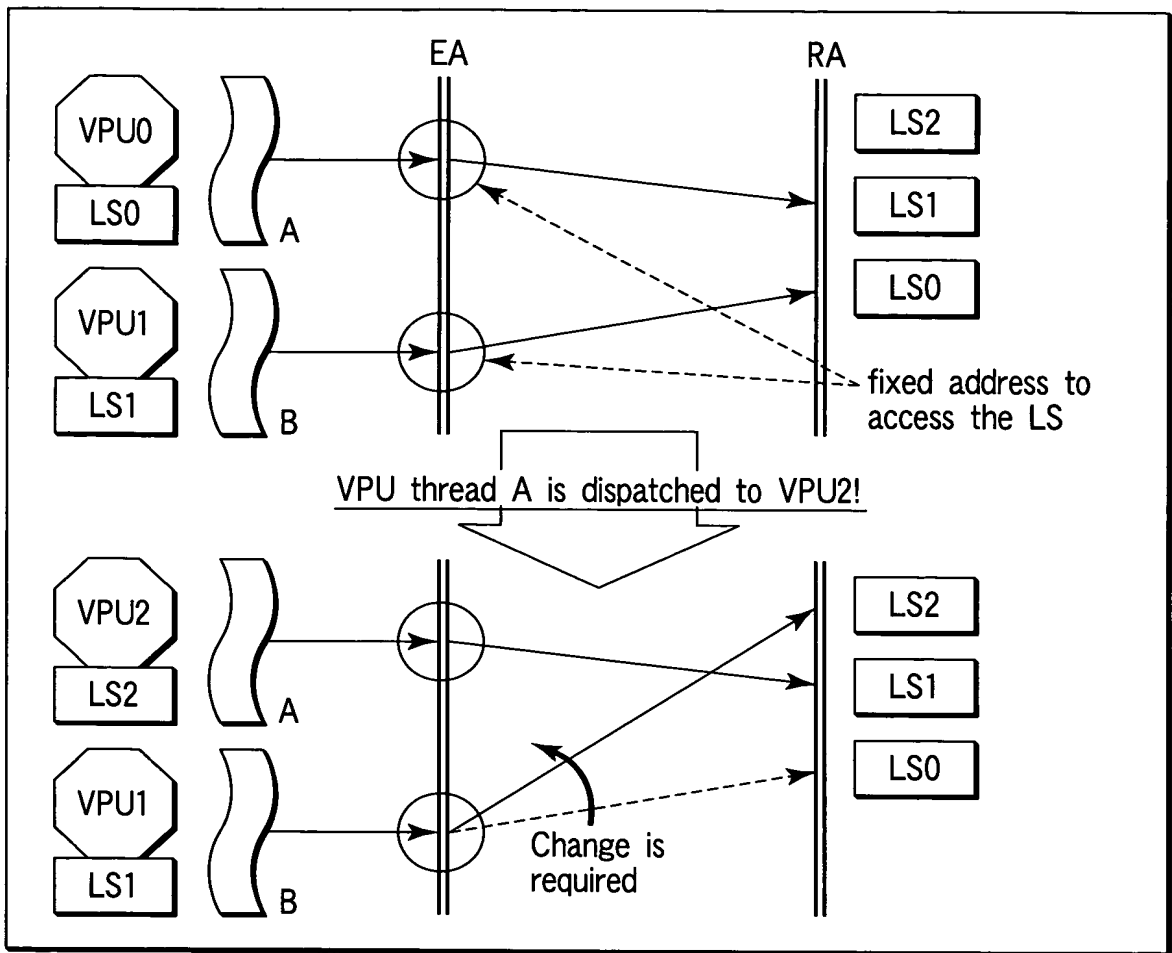


FIG. 32

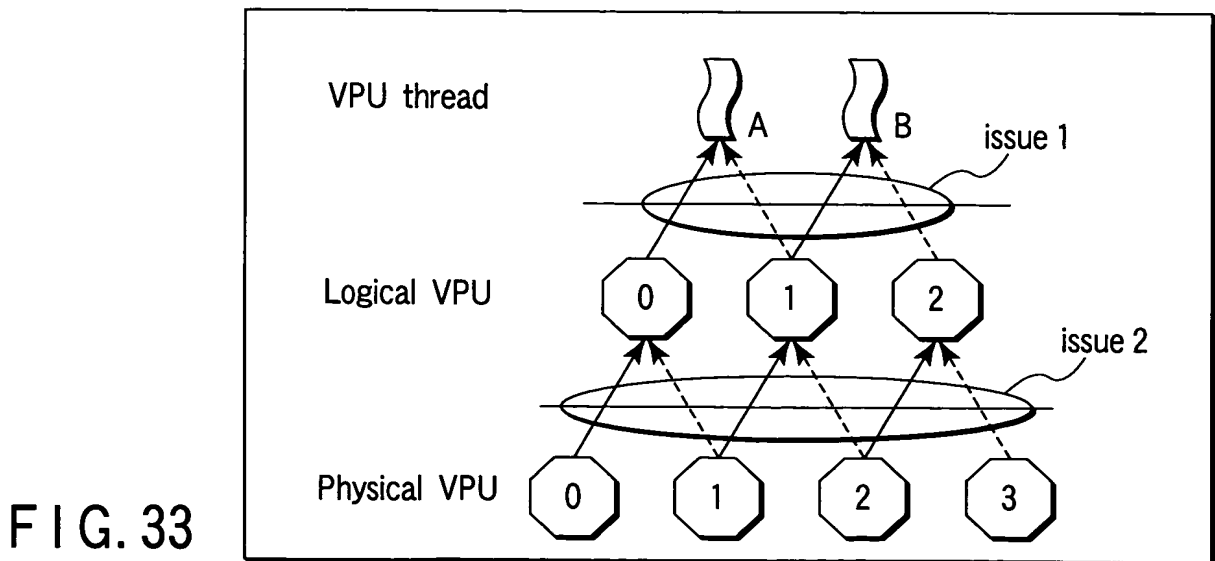


FIG. 33

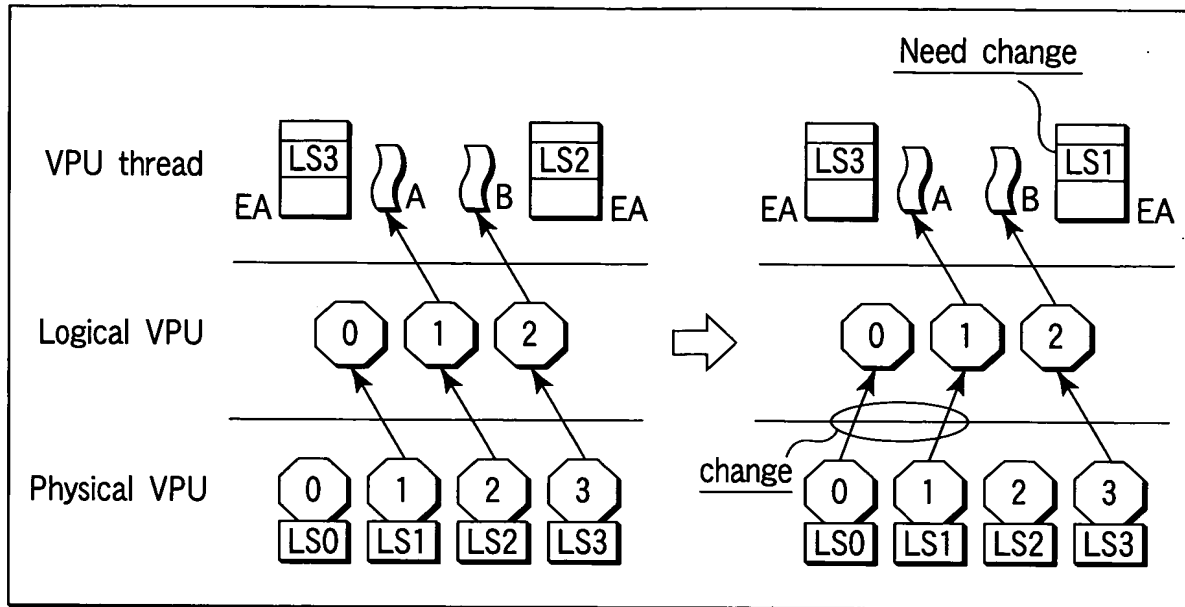


FIG. 34

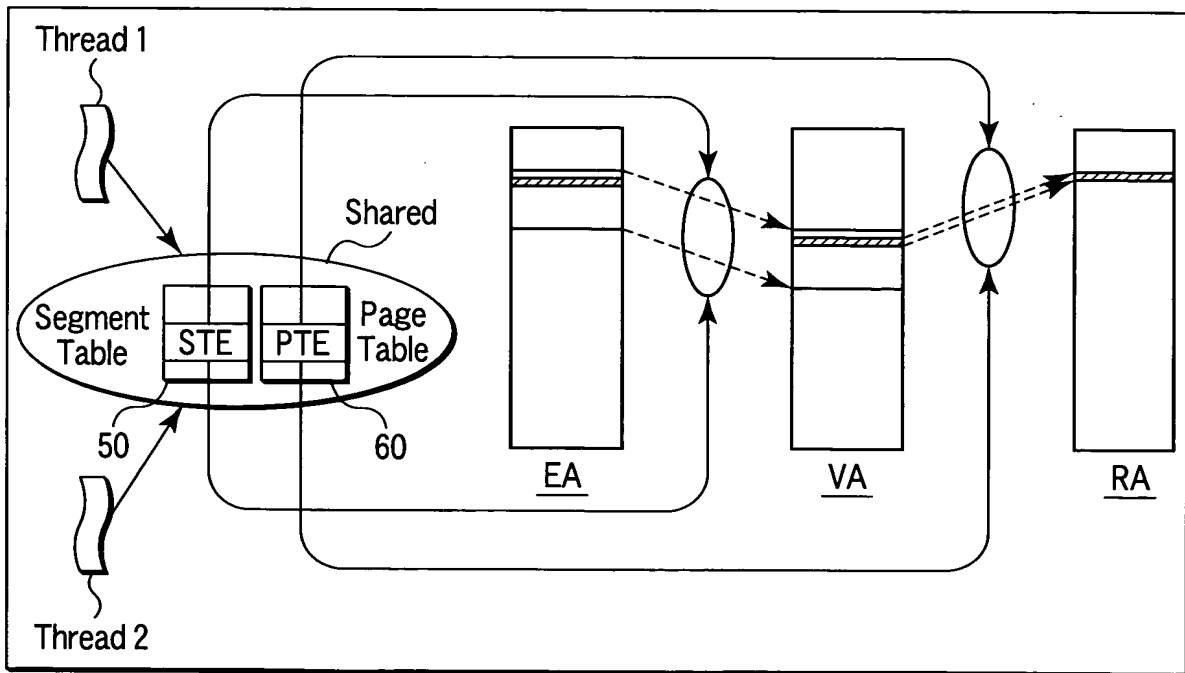


FIG. 35

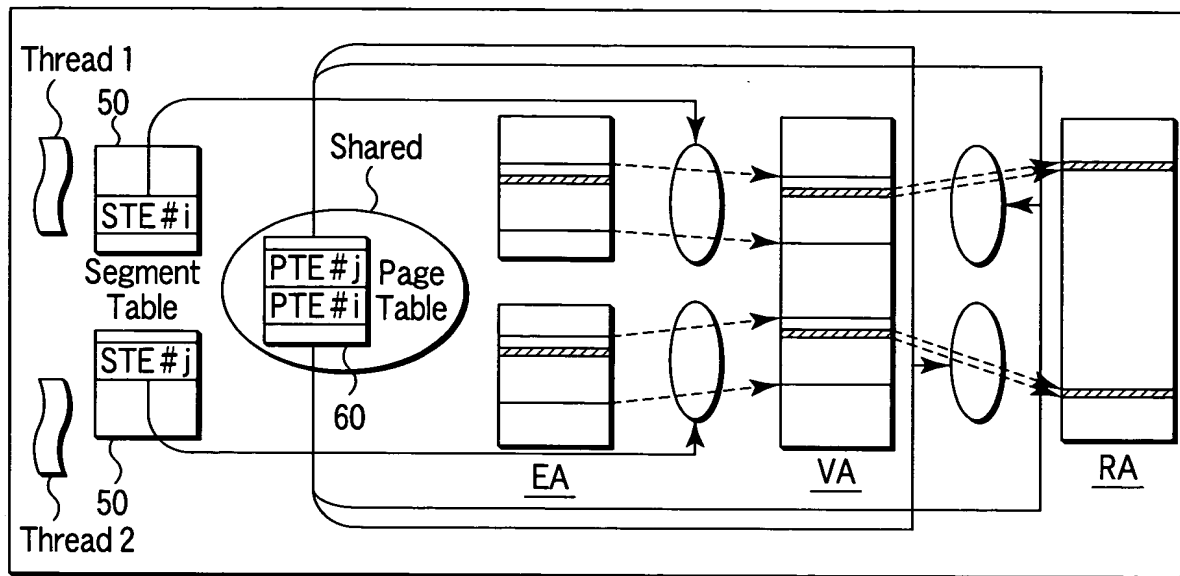


FIG. 36

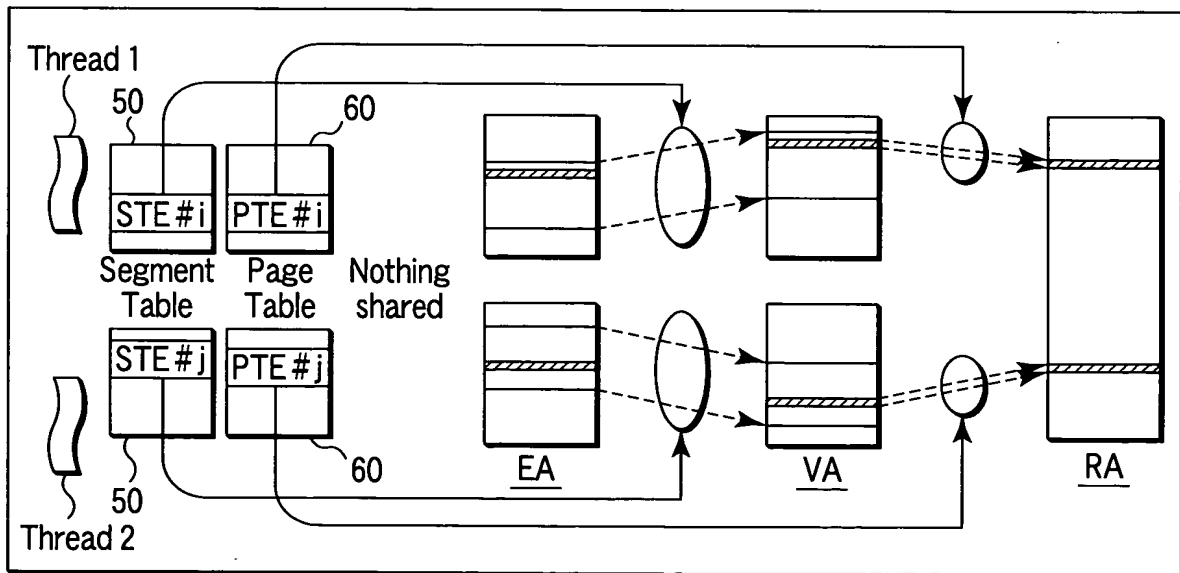
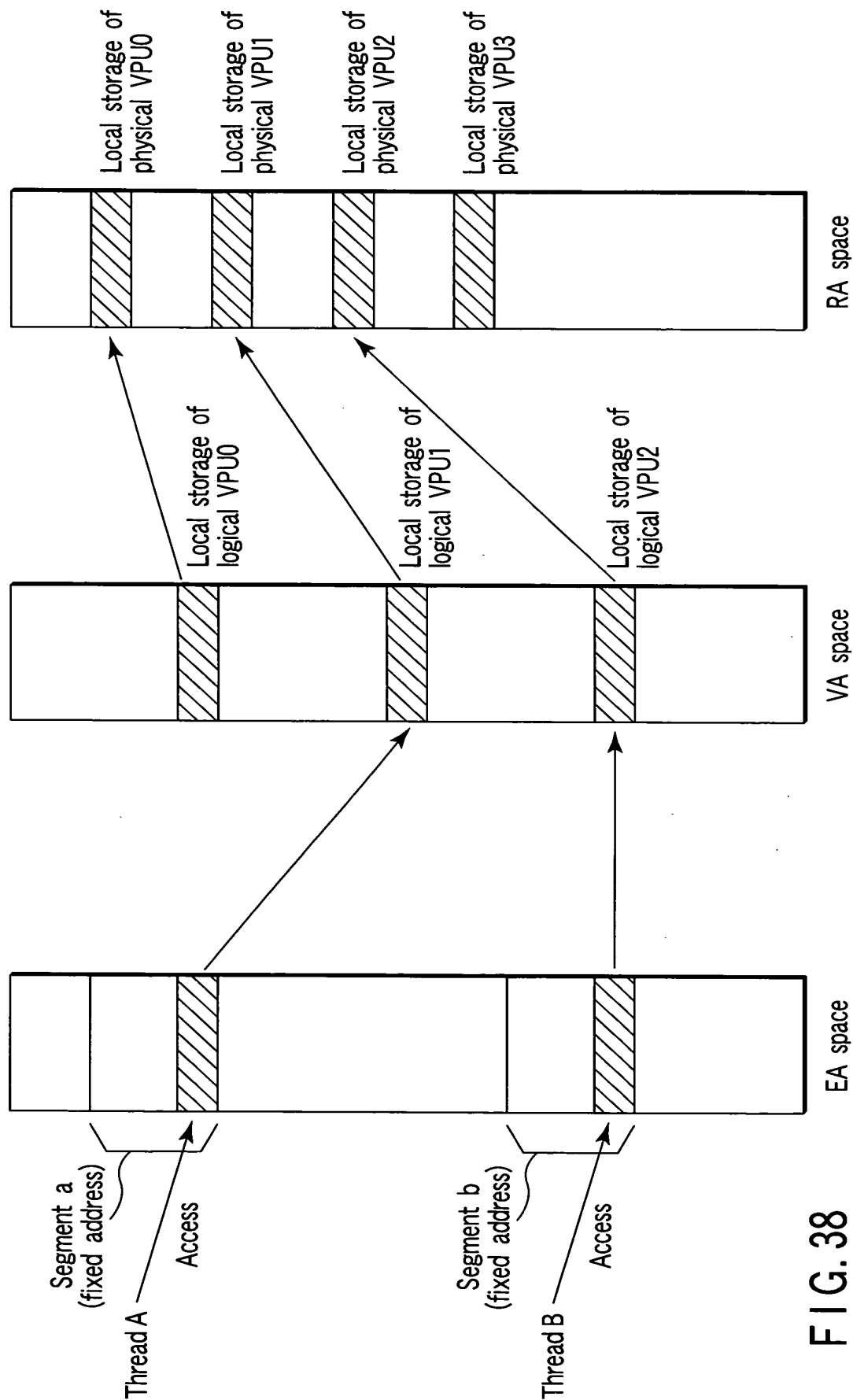


FIG. 37



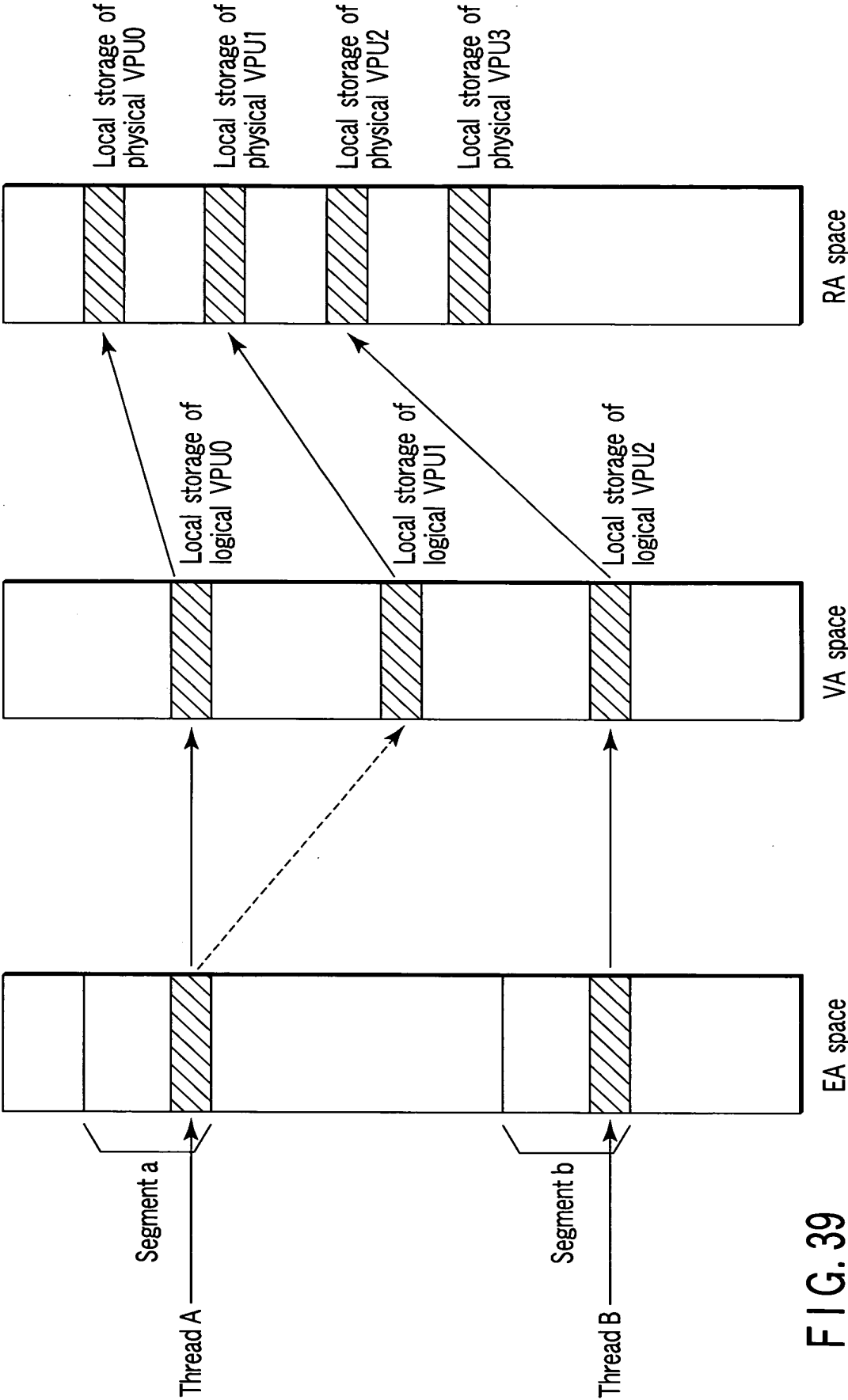


FIG. 39

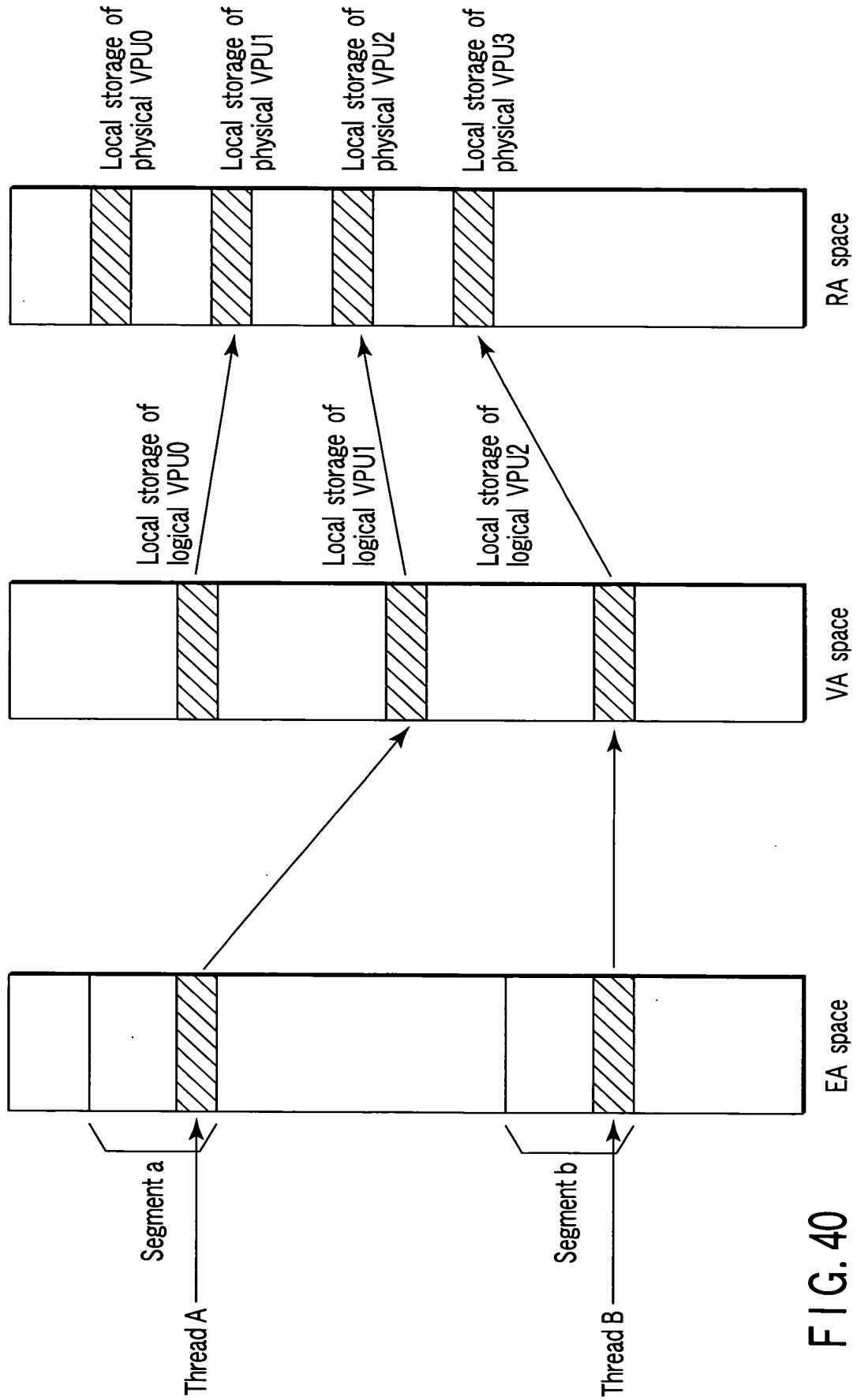
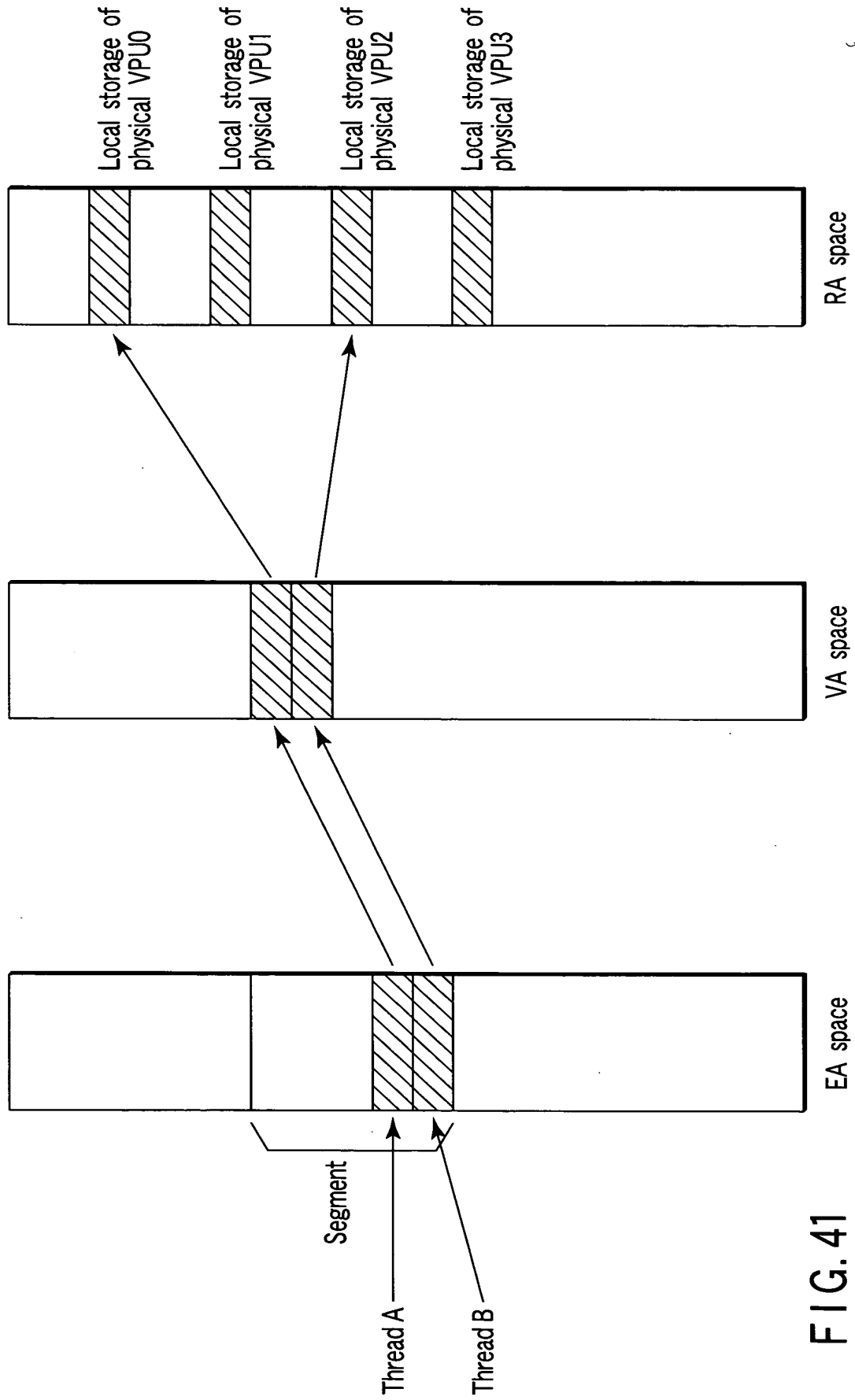


FIG. 40



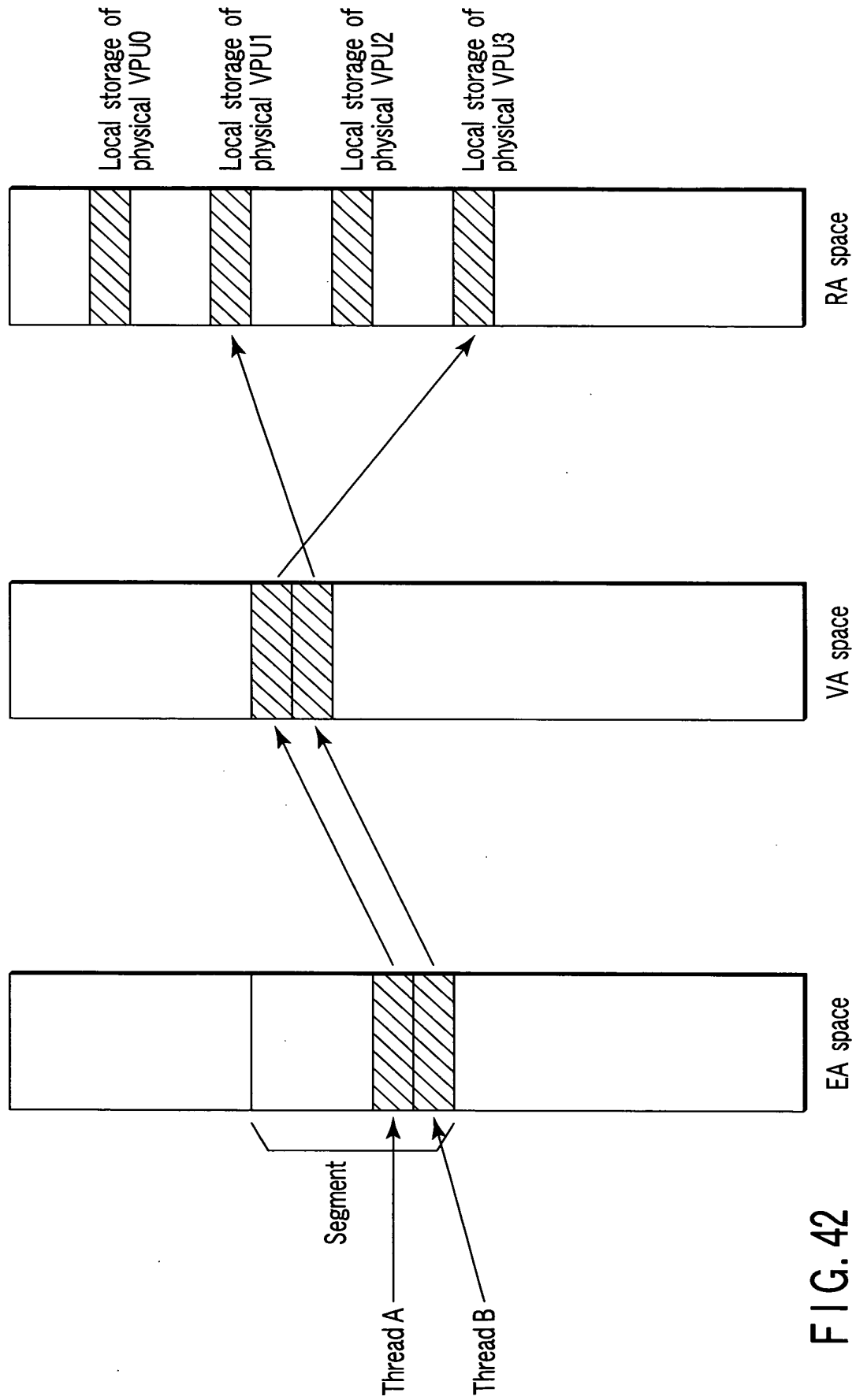


FIG. 42

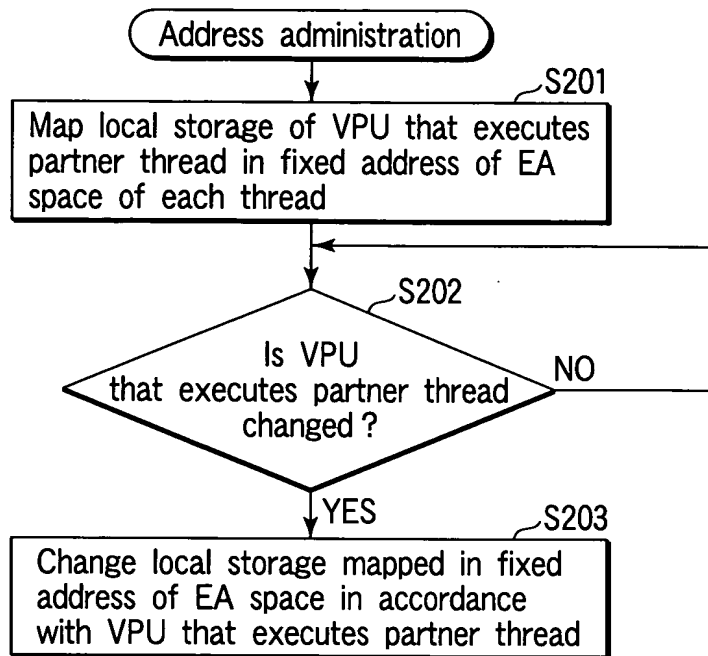


FIG. 43

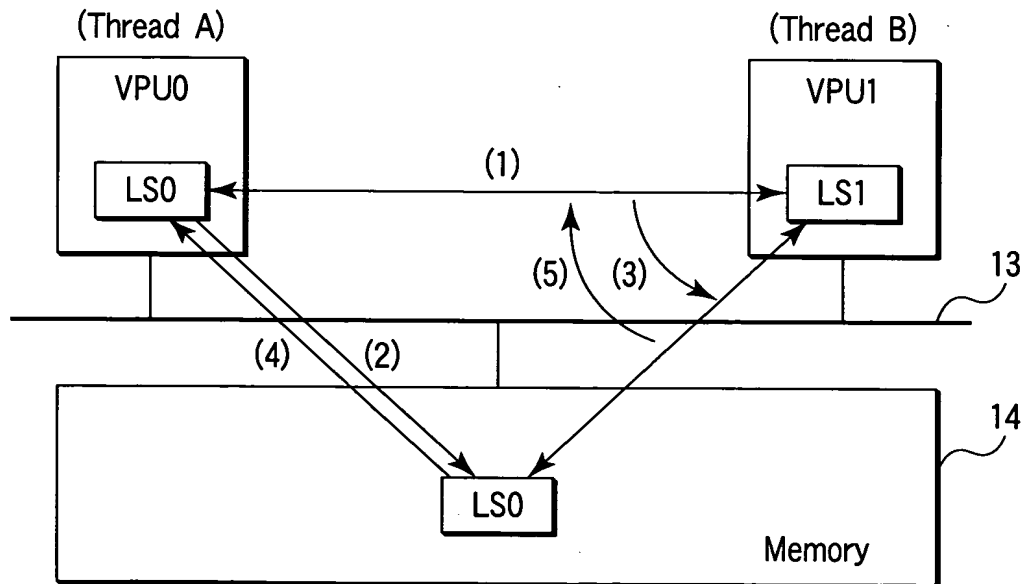


FIG. 44

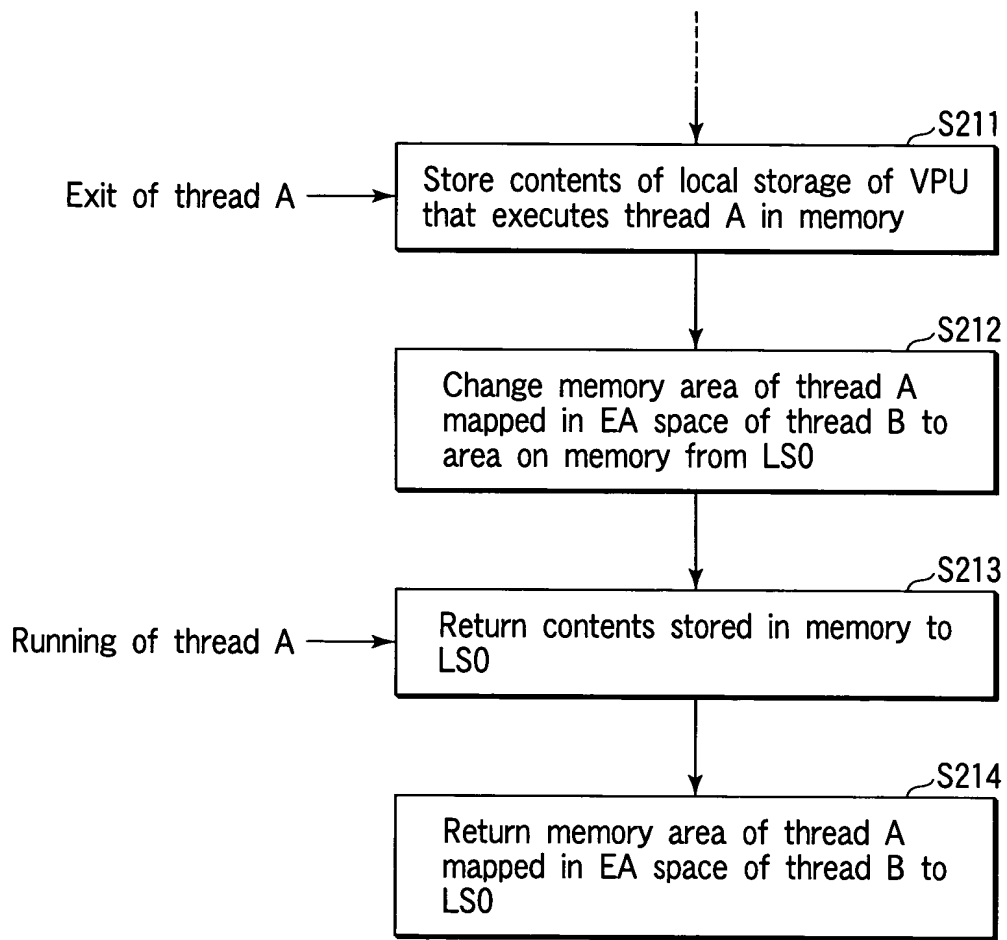


FIG. 45

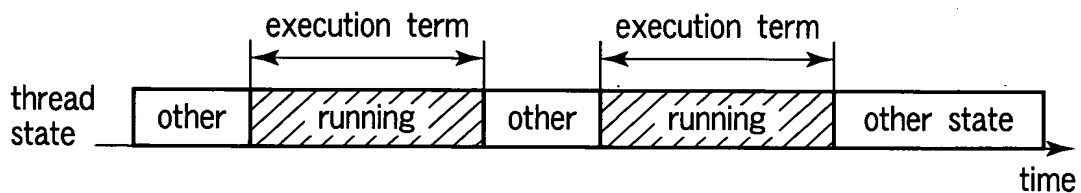
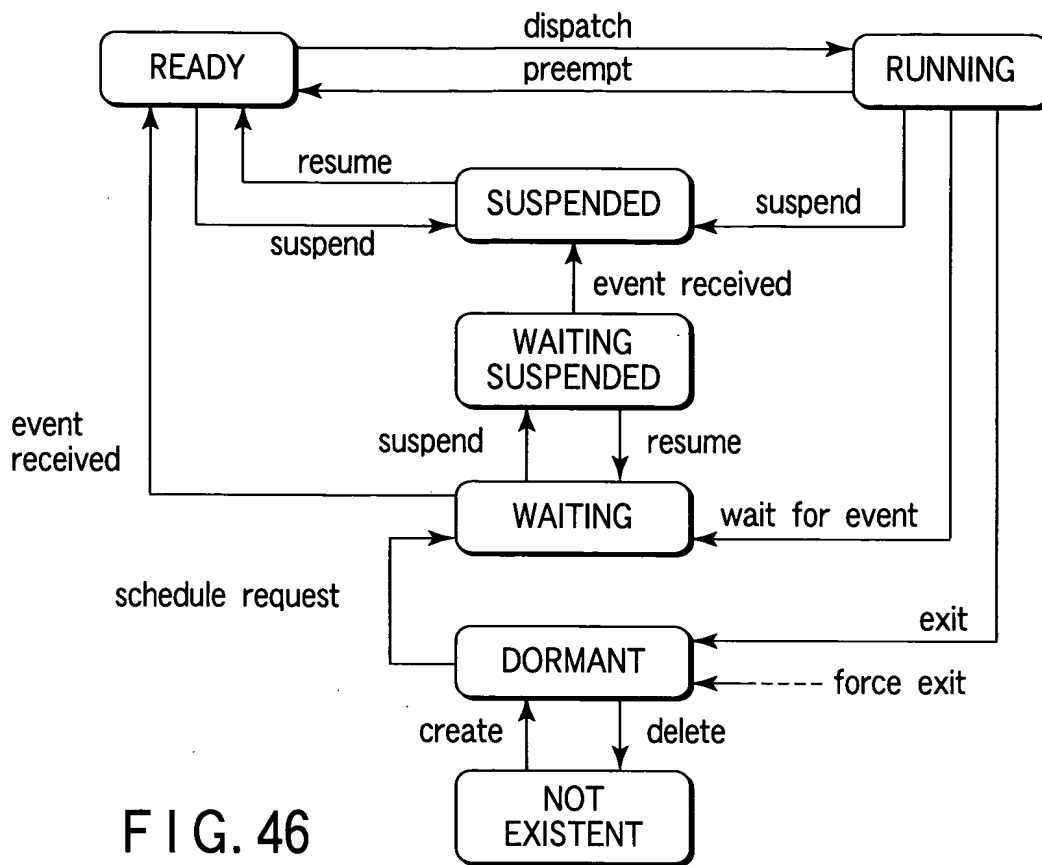


FIG. 47

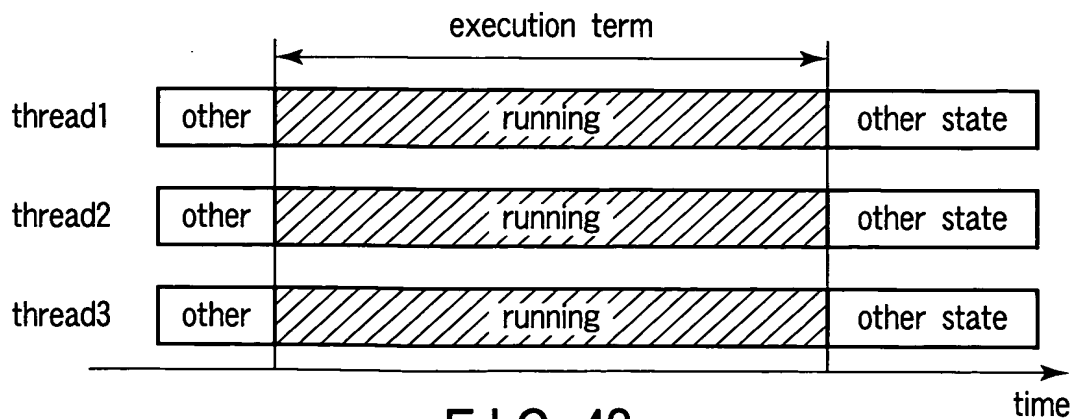


FIG. 48

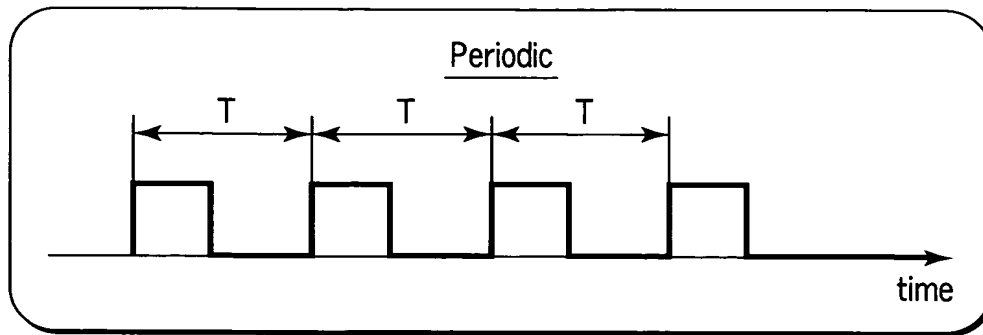


FIG. 49

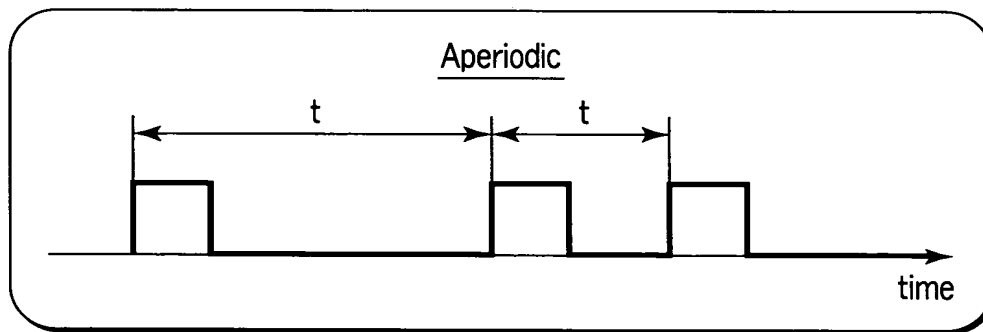


FIG. 50

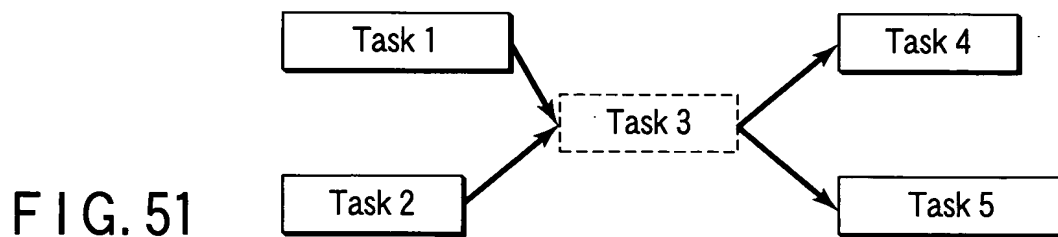


FIG. 51

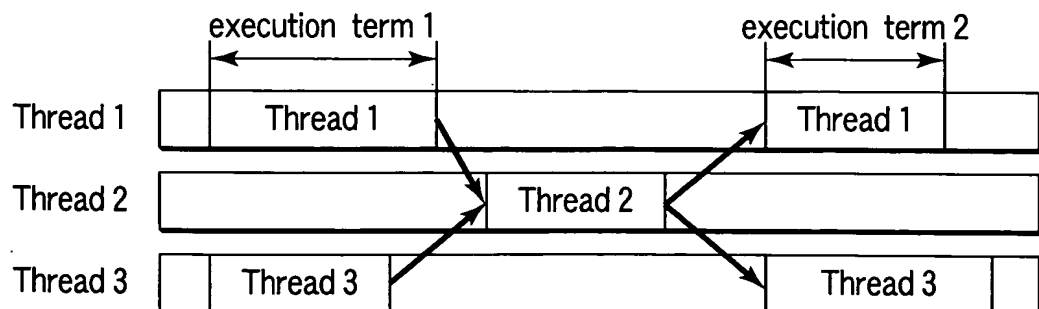


FIG. 52

FIG. 53

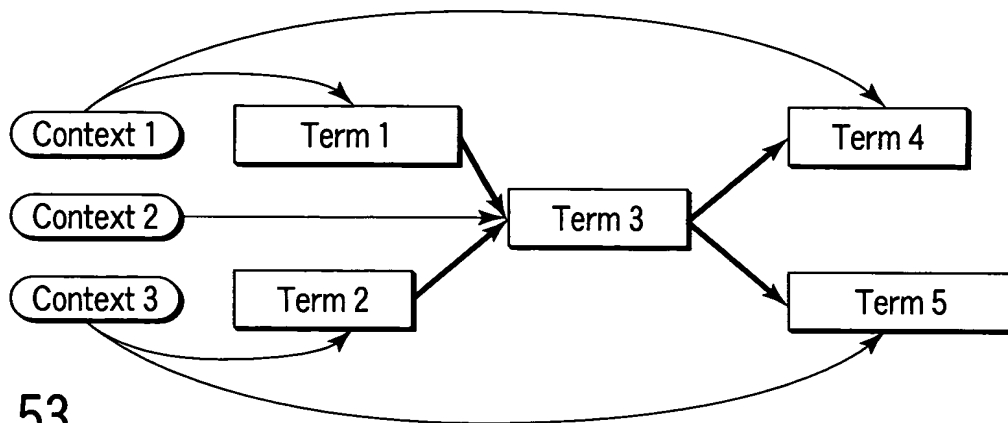


FIG. 54

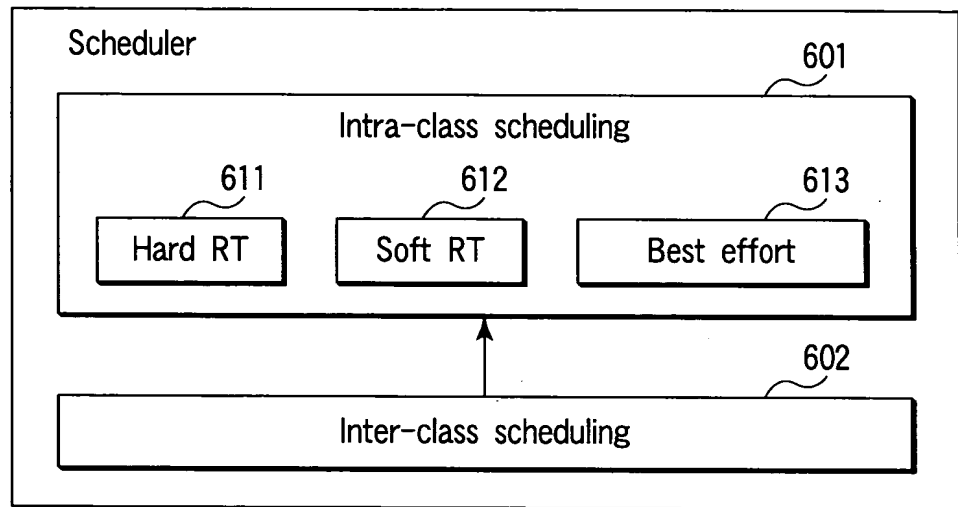


FIG. 55

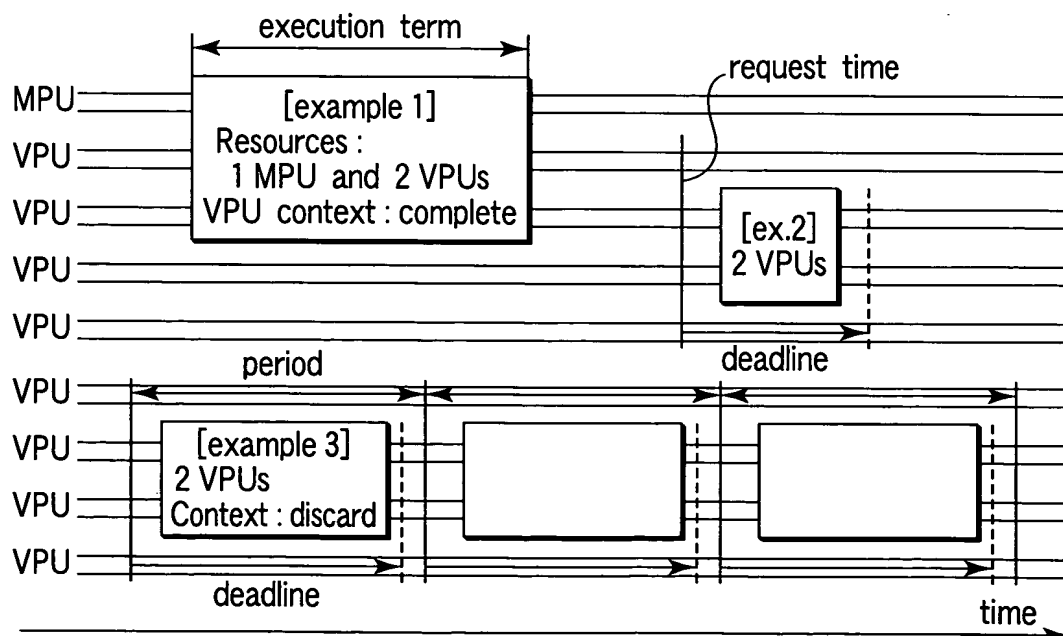


FIG. 56

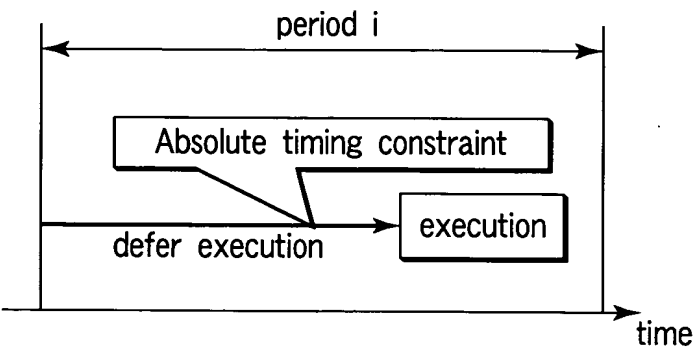


FIG. 57

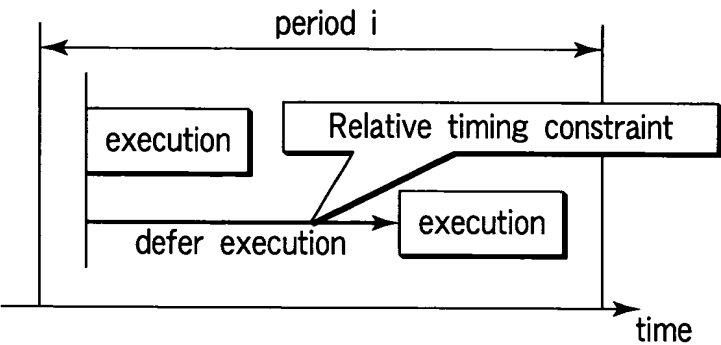
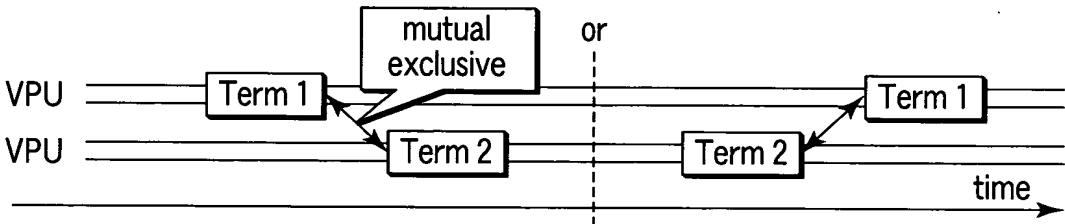


FIG. 58



		Tightly coupled thread group	Loosely coupled thread group
On memory	LS	Can use	Cannot use
	MS	Can use	
Other		Should use hardware primitives	Should use mechanisms provided by VPU Runtime Environment

FIG. 59

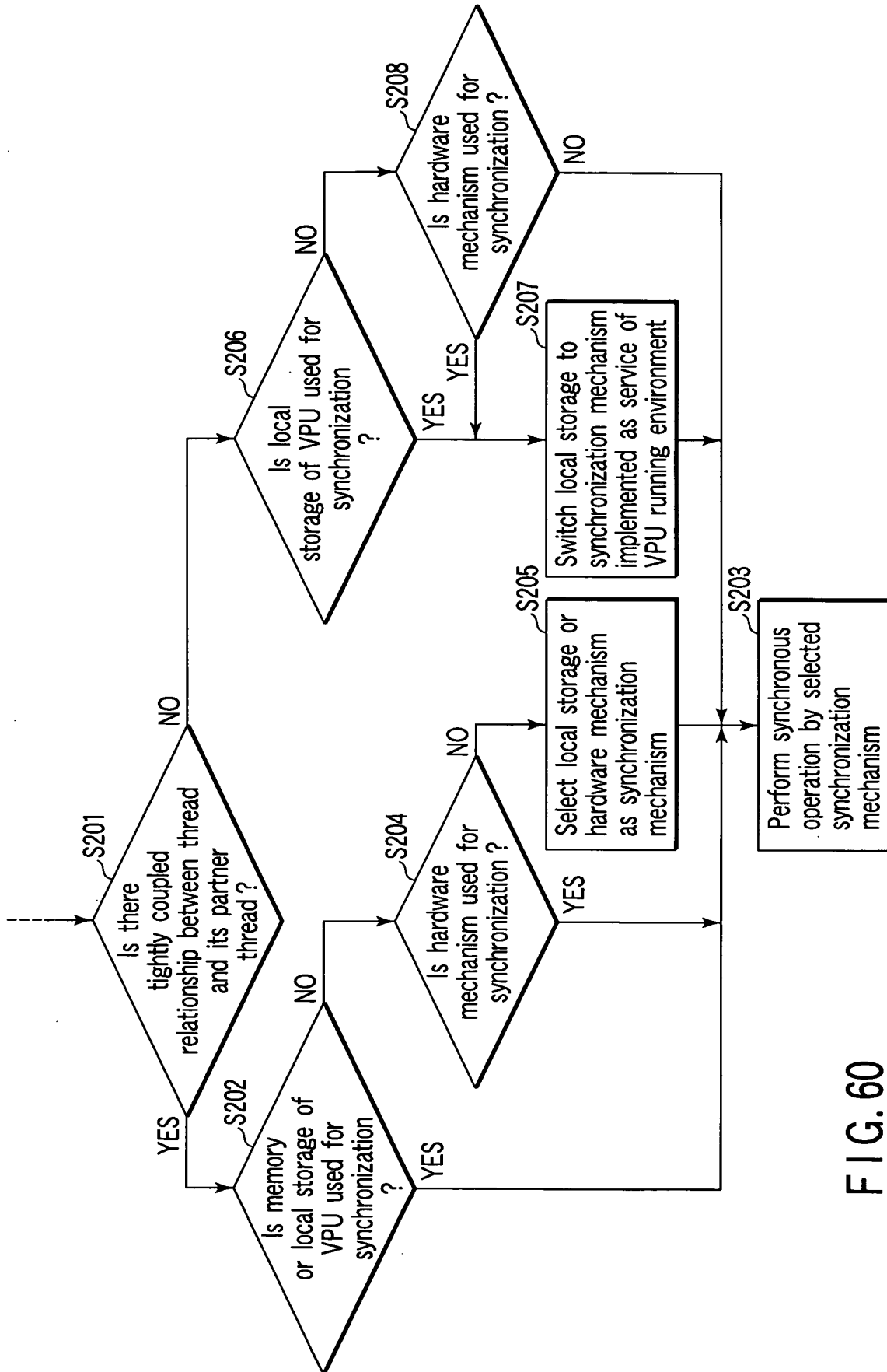
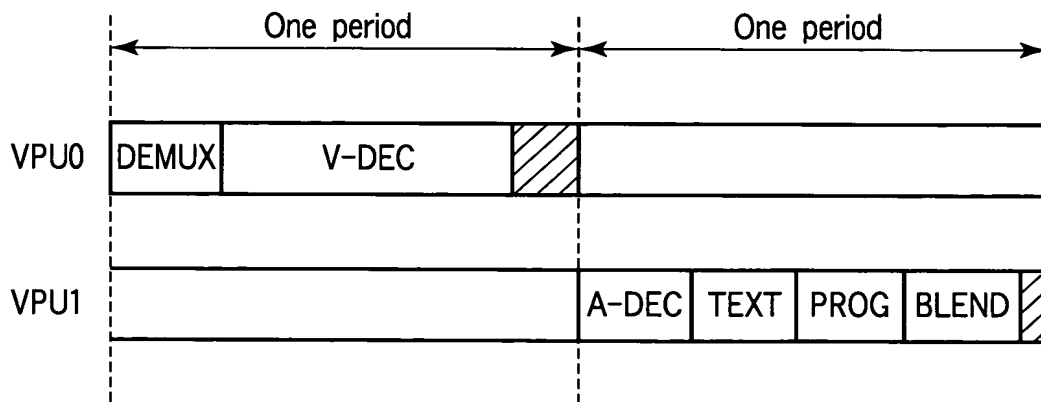
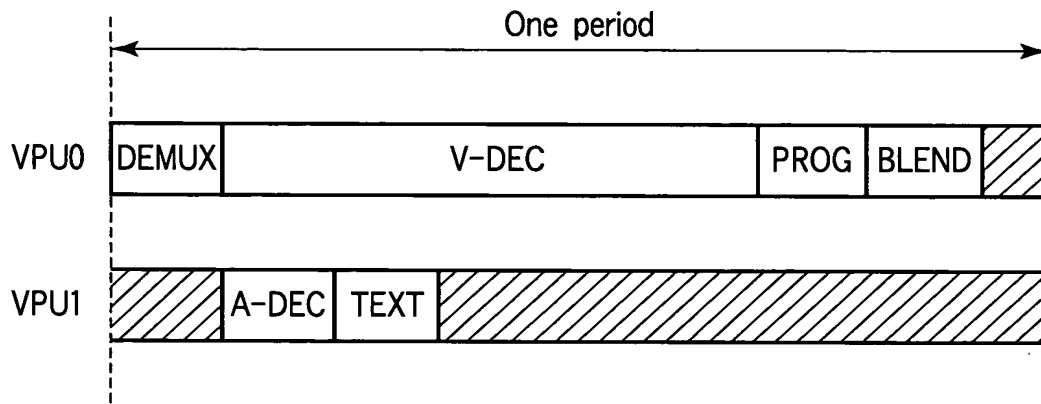
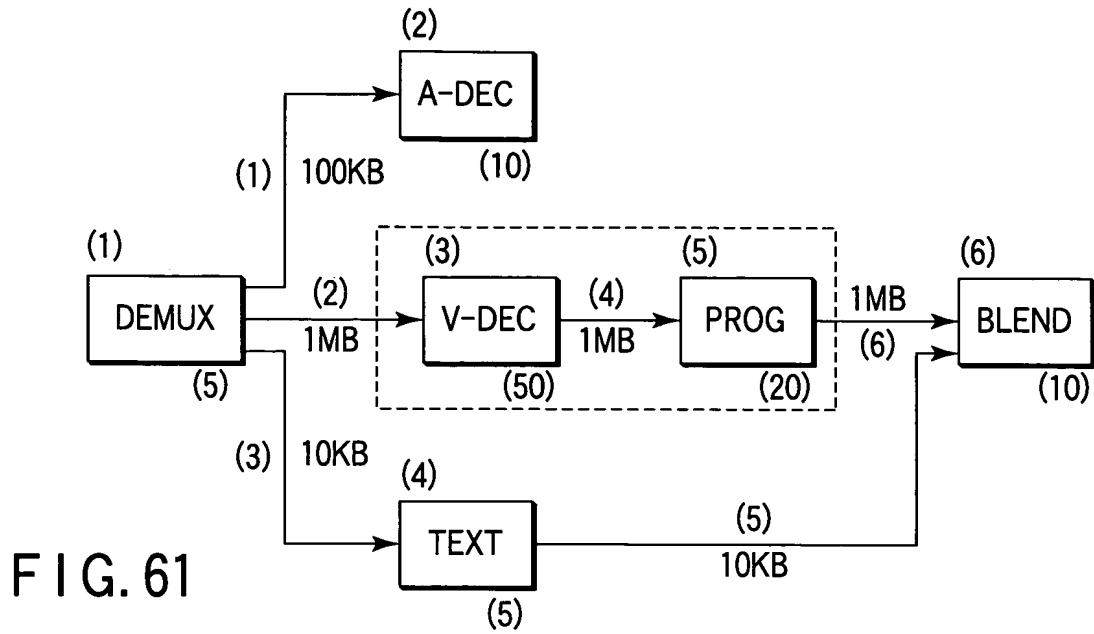


FIG. 60



<u>BUFFER</u>	Id : 1	
Size : 100KB	SrcTask : 1	DstTask : 2
<u>BUFFER</u>	Id : 2	
Size : 1MB	SrcTask : 1	DstTask : 3
<u>BUFFER</u>	Id : 3	
Size : 10KB	SrcTask : 1	DstTask : 4
<u>BUFFER</u>	Id : 4	
Size : 1MB	SrcTask : 3	DstTask : 5
<u>BUFFER</u>	Id : 5	
Size : 10KB	SrcTask : 4	DstTask : 6
<u>BUFFER</u>	Id : 6	
Size : 1MB	SrcTask : 5	DstTask : 6
<u>TASK</u>	Id : 1	Class : VPU,HRT
ThreadContext : DEMUX	Cost : 5	
Constraint : Precede : 2,3,4		
InputBuffer :	OutputBuffer : 1,2,3	
<u>TASK</u>	Id : 2	Class : VPU,HRT
ThreadContext : A-DEC	Cost : 10	
Constraint : Precede :		
InputBuffer : 1	OutputBuffer :	
<u>TASK</u>	Id : 3	Class : VPU,HRT
ThreadContext : V-DEC	Cost : 50	
Constraint : Precede : 5		
InputBuffer : 2	OutputBuffer : 4	
<u>TASK</u>	Id : 4	Class : VPU,HRT
ThreadContext : TEXT	Cost : 5	
Constraint : Precede : 6		
InputBuffer : 3	OutputBuffer : 5	
<u>TASK</u>	Id : 5	Class : VPU,HRT
ThreadContext : PROG	Cost : 20	
Constraint : Precede : 6		
InputBuffer : 4	OutputBuffer : 6	
<u>TASK</u>	Id : 6	Class : VPU,HRT
ThreadContext : BLEND	Cost : 10	
Constraint : Precede : 5		
InputBuffer : 5,6	OutputBuffer :	

FIG. 62

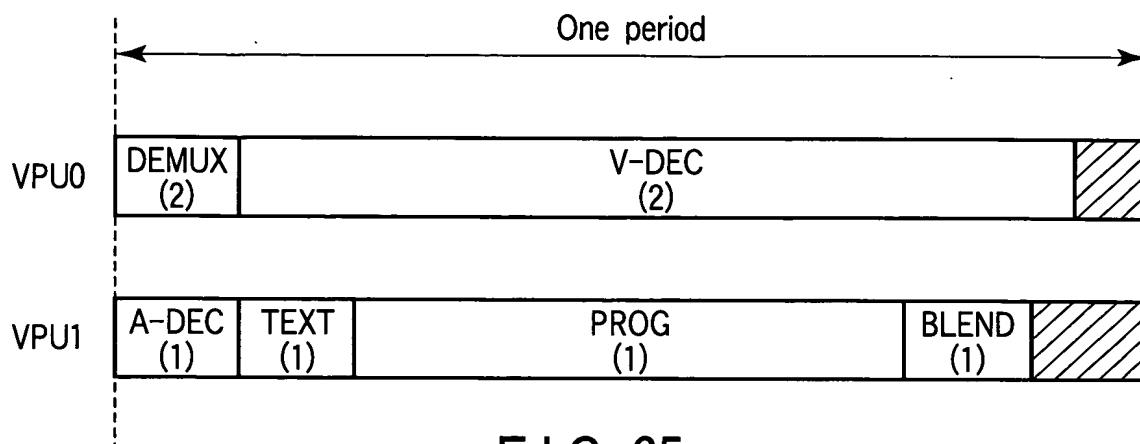


FIG. 65

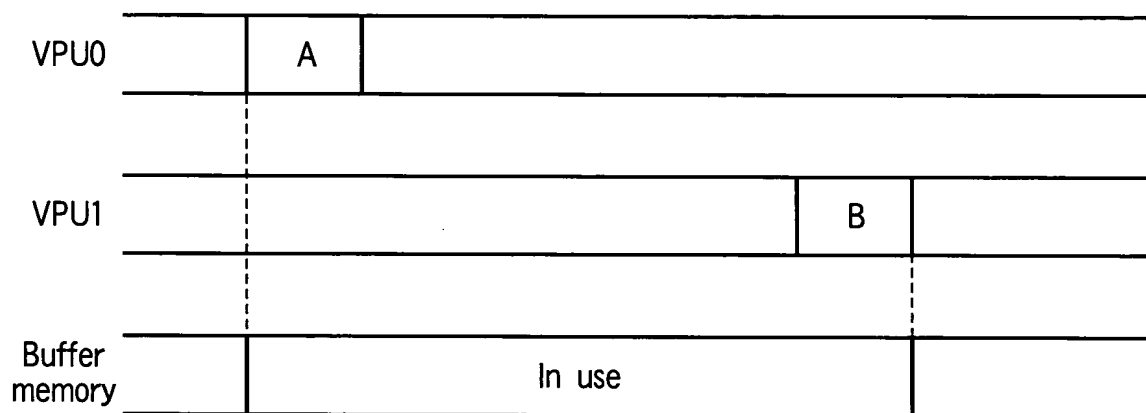


FIG. 66

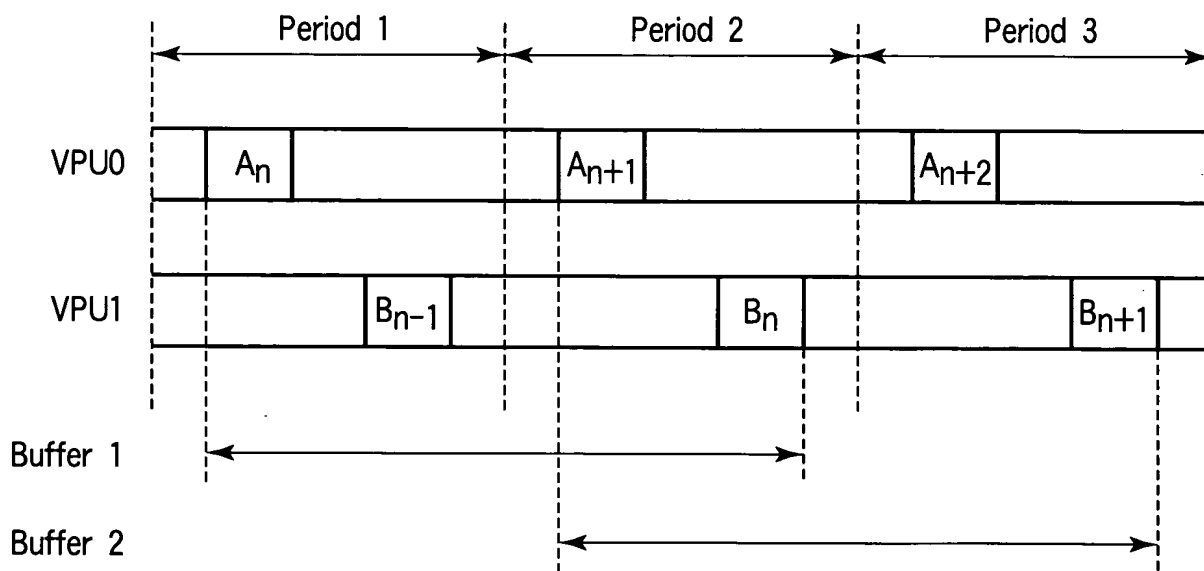


FIG. 67

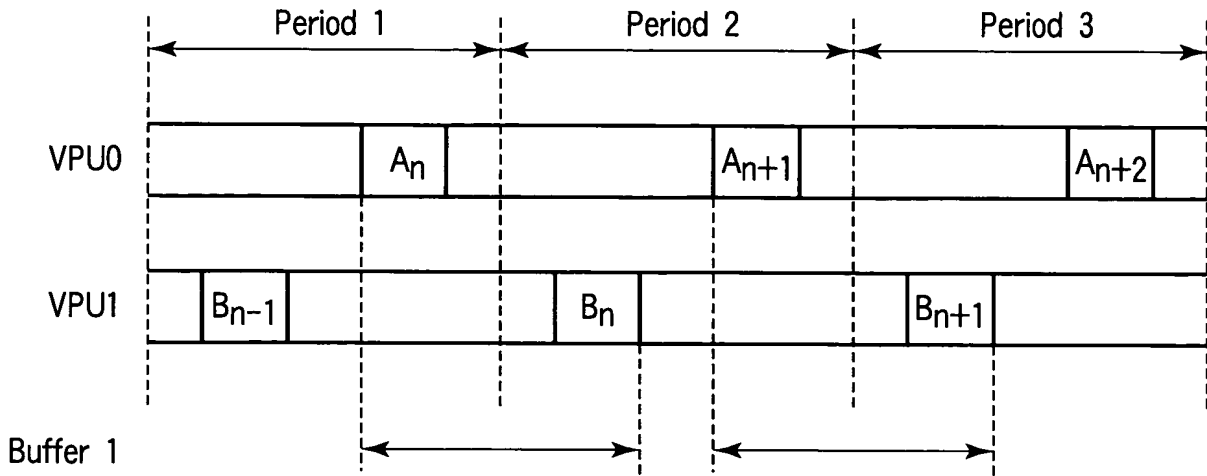


FIG. 68

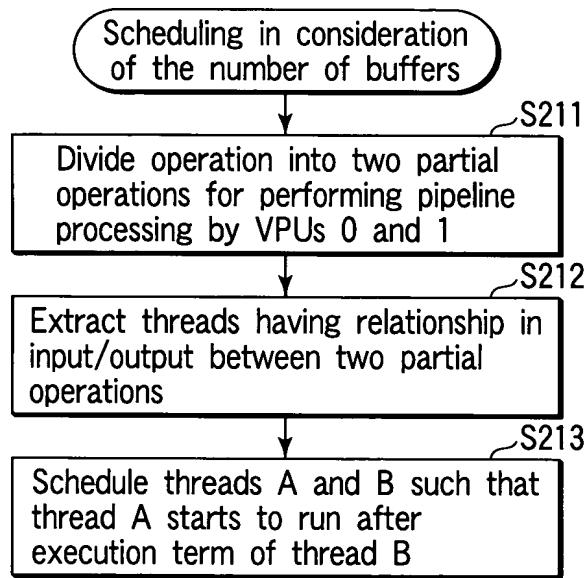


FIG. 69

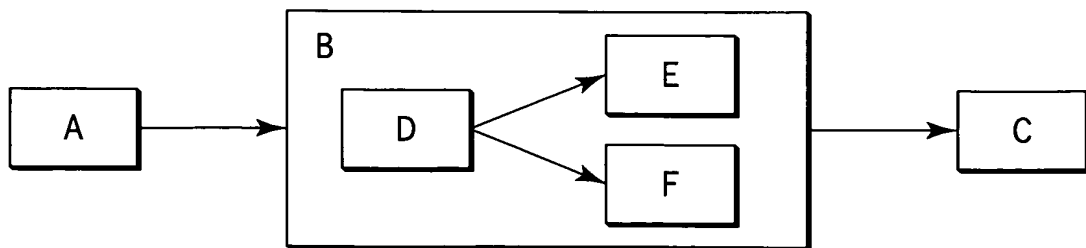


FIG. 70

<u>BUFFER</u>	Id : 1
Size : 100KB	SrcTask : 1 DstTask : 2
<u>BUFFER</u>	Id : 2
Size : 1MB	SrcTask : 1 DstTask : 3
<u>BUFFER</u>	Id : 3
Size : 10KB	SrcTask : 1 DstTask : 4
<u>BUFFER</u>	Id : 4
Size : 10KB	SrcTask : 4 DstTask : 6
<u>BUFFER</u>	Id : 5
Size : 1MB	SrcTask : 5 DstTask : 6
<u>TASK</u>	Id : 1 Class : VPU,HRT
ThreadContext : DEMUX	Cost : 5
Constraint : Precede : 2,3,4	
InputBuffer :	OutputBuffer : 1,2,3
<u>TASK</u>	Id : 2 Class : VPU,HRT
ThreadContext : A-DEC	Cost : 10
Constraint : Precede :	
InputBuffer : 1	OutputBuffer :
<u>TASK</u>	Id : 3 Class : VPU,HRT
ThreadContext : V-DEC	Cost : 50
Constraint : Precede : 5	TightlyCoupled : 5
InputBuffer : 2	OutputBuffer :
<u>TASK</u>	Id : 4 Class : VPU,HRT
ThreadContext : TEXT	Cost : 5
Constraint : Precede : 6	
InputBuffer : 3	OutputBuffer : 4
<u>TASK</u>	Id : 5 Class : VPU,HRT
ThreadContext : PROG	Cost : 50
Constraint : Precede : 6	TightlyCoupled : 3
InputBuffer :	OutputBuffer : 5
<u>TASK</u>	Id : 6 Class : VPU,HRT
ThreadContext : BLEND	Cost : 10
Constraint : Precede : 5	
InputBuffer : 4,5	OutputBuffer :

FIG. 71

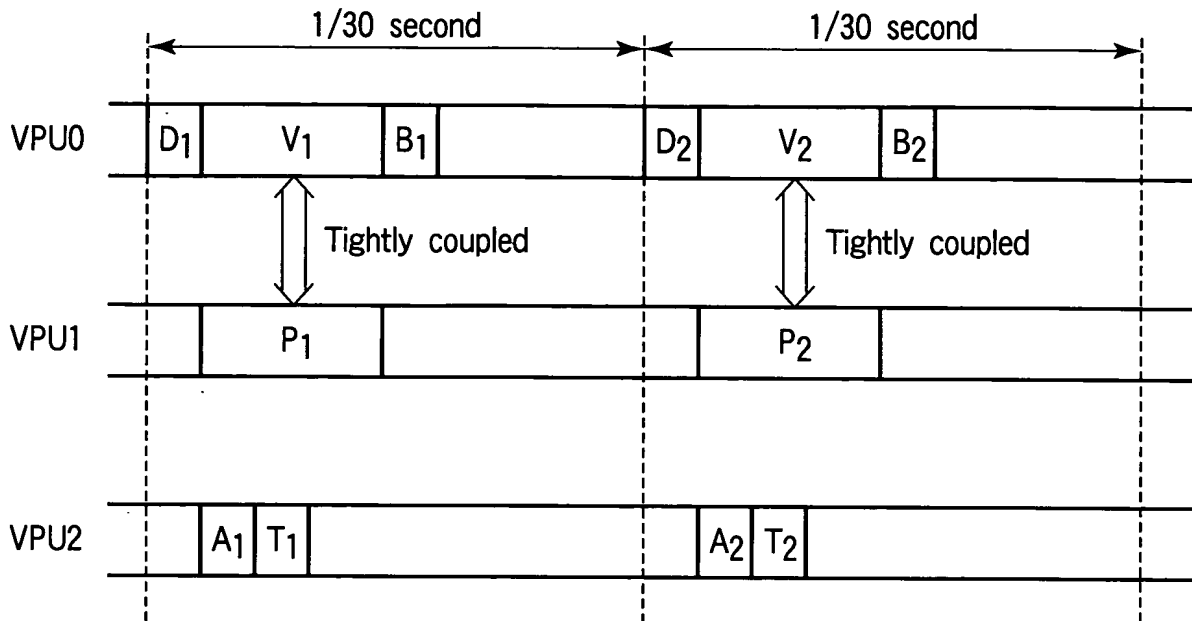


FIG. 72

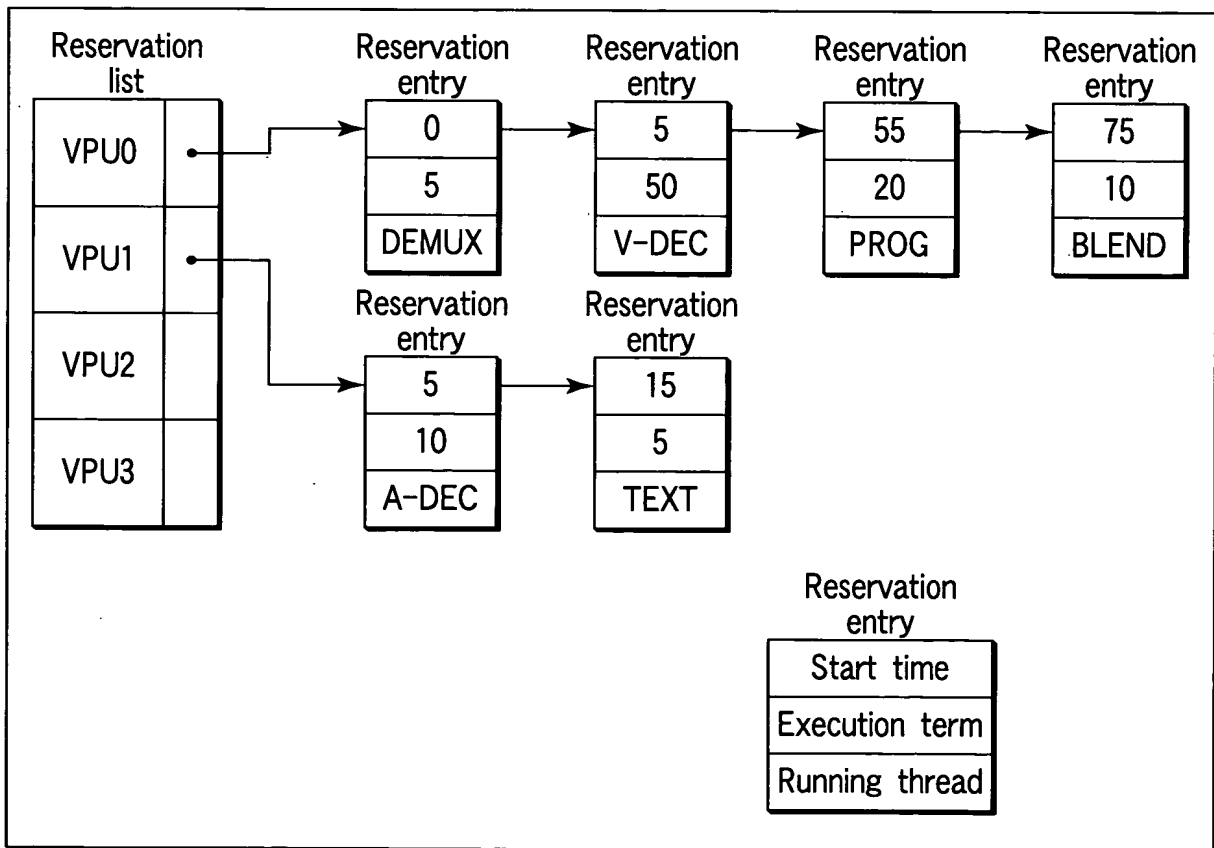


FIG. 73

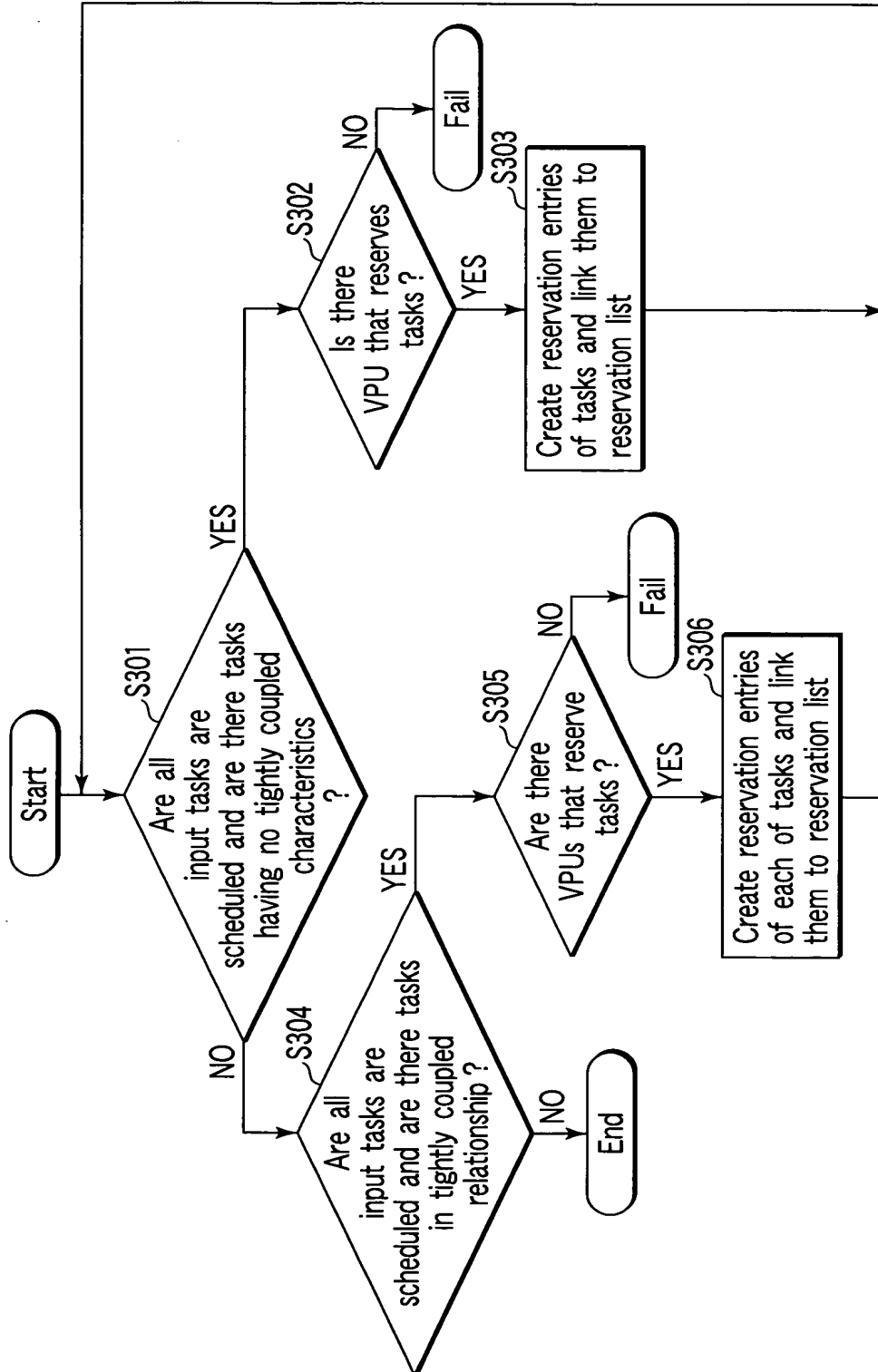


FIG. 74